MODIFIED PRE-CHARGE FREE TCAM CELL FOR LOW POWER APPLICATIONS

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ABSTRACT:

To speed up location access and data association in modern systems hardware search engines are replaced by software algorithms. Due to its parallel search accessibility Content addressable memory is one of the hardware search engines. Ternary CAM based tables are employed.Ternary Content addressable memory (TCAM) gives high speed but also consumes high power. For higher search speed application and low power applications so pre charge free TCAM is proposed. Pre charge-free CAM is used to reduce the power and increase the search speed. These are suitable for both high-search speed and low power consumption applications. Basically, these are used for packet forwarding in network routers. This design is simulated using Tanner tool.

KEYWORDS: Matchline,TCAM, PF-TCAM, Precharge

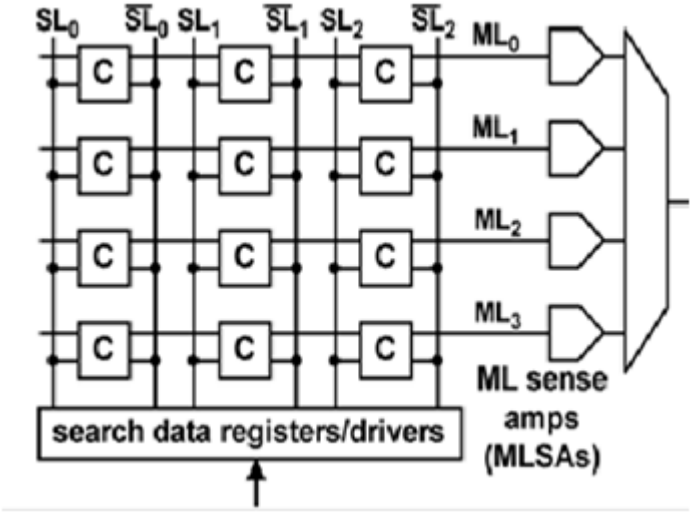
INTRODUCTION

Battery operated portable devices such as smart phones,laptops, personal computers and similar electronic computing devices are commonly used appliances in everyday life.Regular usage of these devices is based on MAC table that provides connectivity from one device to another. On a broader level between users at different locations, internet connectivity is becoming the main interface (the backbone). Internally,MAC tables comprise of TCAMs as memory module to improve performance of table access. All these primary electronic appliances consist of cache memory internally between processor and main memory to improve the access speed oftask execution. There is a high probability of cache miss in conventional direct-mapped cache due to continuous refresh ofcache memory.

CAM fast operation due to the content of all the contents stored in the memory of the parallel search operations in a single clock cycle. That is, CAM simultaneously retrieves content stored in the memory of all input words. However, this would result in high power dissipation of the CAM. Therefore, since the comparison operation and a large number of parallel CAM search operation, the power consumption is always a problem CAM design of major concern.

A connection model of two different networks (for example, between a wired network and wireless network) using a network bridge is illustrated in Fig. 1 to show the importance of CAM tables. Not only does the appliances require to meetdaily utilization but also they demand reliable operation within internet traffic with low-power as well as high-performance table access. This is where TCAM plays a significant role in achieving performance goals. We introduce first ever precharge free TCAM cell for meeting performance requirements of various applications where data association is employed. The limitation of precharge phase reduces the total number of cycles and doubles the search rate probability of cache despite energy efficiency improvement.

TCAM is a memory element in which the information is storedin rows and search happens in parallel. Content addressable memory, takes content as an input and gives address as an output If stored data matches with the search data then it gives address in which the data stored. A match or mismatch information is accessed by the sense amplifier. Every TCAM cell in a wordline is connected to a common match line (ML). Initially all match lines are charged to high voltage. ML value maintains at high voltage if there is a match. . TCAMs are used in a number of routing applications and hardwares such as network router, cache memories.



LITERATURE REVIEW:

[1]TelajalaVenkataMahendra and his team proposed This paper introduces a precharge-free searching approach in ternary CAM as an alternative solution to precharge type TCAMs. Absence of precharge cycle in the proposed precharge-free TCAM (PF-TCAM) reduces evaluation time by50%, which can enormously be useful in various applications involving search, association and computation. The introduced TCAM performs search in HALF clock cycle while existing TCAM designs performs search in single clock cycle.

[2]The proposed scheme avoids the PRE phase and nullifies the dependence between CAM cells in a word due to the self control scheme. This gives an advantage to perform more searches within a stipulated time.

[3]Content Addressable Memory is the hardware for parallel look up search. The parallel search scheme promises a high speed search operation but at the cost of high power consumption. Parallel NOR and NAND-TYPE CAMs are suitable for high search speed and low power consumption applications, respectively.

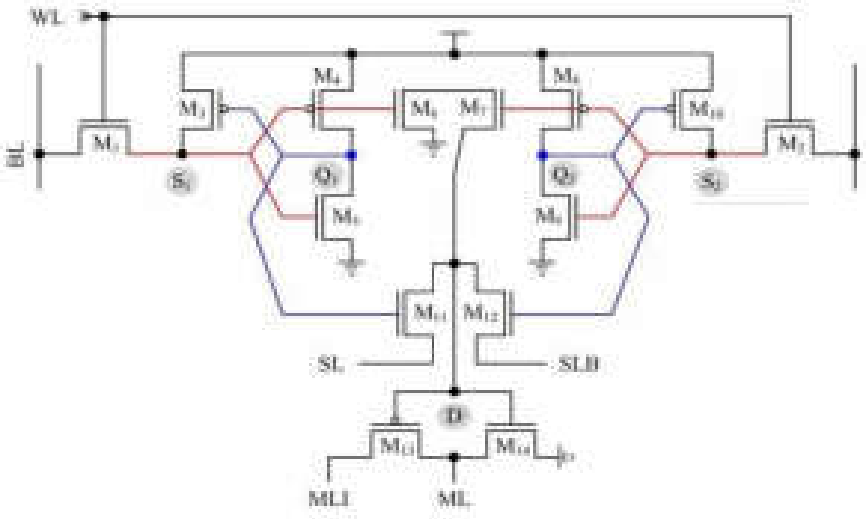
[4]The Proposed design of large-capacity content addressable memory (CAM).A CAM is a memory that implements the look up-tables function in a single clock circuitry.

EXISTING CIRCUIT

A complete ternary approach is introduced that can provide masking for variety of applications. For masking,local and global mask drivers are not required in proposed design because it is done through data write/content search drivers: it minimizes design area and decreases power in overall system.

The proposed work reduces the evaluation time by 50 percent compared to existed works on TCAM and resulted as a high search rate engine.

Multiple search analysis on TCAM and Monte-Carlo(MC) sampling method have been carried out on the proposed design to test its robustness besides providing the performance improvement.



METHODOLOGY:

The nodes (Q1,Q2) are used for charge storage; those store complementary data when the written information is 0 (or) 1.The soft storage nodes (S1 and S2) help in maintaining the charge at Q1 and Q2. Since the soft storage nodes are charged through the pull-up transistors (M3 andM10), in either state of the written value, they don't change their own state over time. Transistor pair M11 & M12 performs the comparison (XOR) operation among (Q1, Q2) and searchlines (SL, SLB). Whenever the search key matches with the stored contents, then searchlines pass a LOW logic tothe decision node (D) through transistor M11 (or) M12 and it turns ON the transistor M13 to pass previous cell ML state(MLI). Otherwise, M14 passes LOW logic to the matchline. Logic '1' on ML represents match state whereas'0' represents a mismatch state. The introduced ternary structure of the PF-CAM adds value to suit bit-level local masking and search enabled global masking, which are as follows:

• Local masking: When a bit-level match is required to be performed, nodes Q1 and Q2 are charged to LOW state, which turns OFF transistors M11 & M12 to avoid XOR comparison operation. Simultaneously, local masking pair(M6 and M7) turns ON to pass LOW logic. It forces the matchline state to match.

• Global masking: Performing a global masking is achieved by pulling the searchline pair (SL and SLB)down in entire memory of that column. It allows the decision node to charge down through either of searchline pass transistor (M11 or M12) since one of the storage nodeis HIGH. One and only exception can be found whenboth storage nodes are discharged (Q1 = Q2 = 0). This isa likely event but only when the cell is masked locally.In either scenario, input MLI is passed to the subsequent cell for decision

PROPOSEDCIRCUIT

The proposed architecture power consumption is less compared to existing design shows the suggested TCAM cell. The ternary encoding of suggested cell is similar to traditional cell. Loading data into TCAM cell is possible by making write enable is active. E and F transistors are in On condition while write enable in high state. Therefore, A and B values will enters into corresponding SRAM cells.

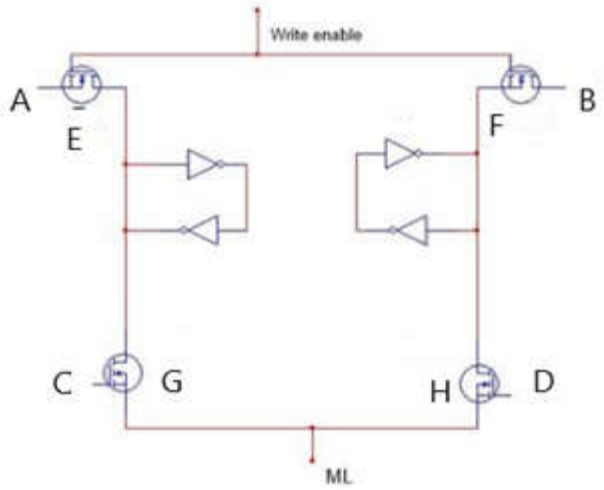


Fig-3 Proposed PF TCAM Cell

METHODOLOGY:

If E = 0 and F = 1 means logic '0' is kept in TCAM. When SL = 0 and = 1 TCAM searches for logic'0'. Hence T3 is OFF and T4 is in On state. Therefore, ML voltage value is at logic '1' because F is at logic '1'. It indicates match. Similarly, search for logic '1' is possible by keeping SL = 1 and = 0 . Here T3 transistor is On and transistor T4 is in OFF state. Here, ML value is at logic '0' because E is at logic '0'. In the same way, logic '1' is kept in cell by keeping E is at logic'0' and F is at logic'1'. It shows mismatch. ML Pre charging is not required here. ML logic value is decided by input logic values. By using the suggested CAM cell a new architecture is proposed. The proposed TCAM without precharge phase

SIMULATIONS AND RESULTS:

In this paper, we have introduced precharge free ternary TCAM by eliminating unnecessary matchline precharge prior to search which is present in existed works.

The proposed TCAM performs search in half clock cycle as it does not requires the matchlines to be precharged at any point of time where as existing works on TCAM performs search in one or more clock cycles.

Performance parameters of the proposed PF-TCAM are analyzed through a random search vector of 1 bit on a 1 bit macro designed using Tanner Tool 45-nm CMOS technology. In order to verify the performance efficiency, post-layout simulations of the proposed TCAM have been compared over the same simulations of conventional TCAM and a compact TCAM of same macro size by supplying 1 V under room temperature. Proposed TCAM can perform search reducing the search cycle requirement by half by achieving better energy efficiency with an area overhead of 1

transistor / TCAM cell compared to compact TCAM with no necessity of any extra control circuits toremove ML precharge. The results, discussions and comparison presented in the paper are of same.

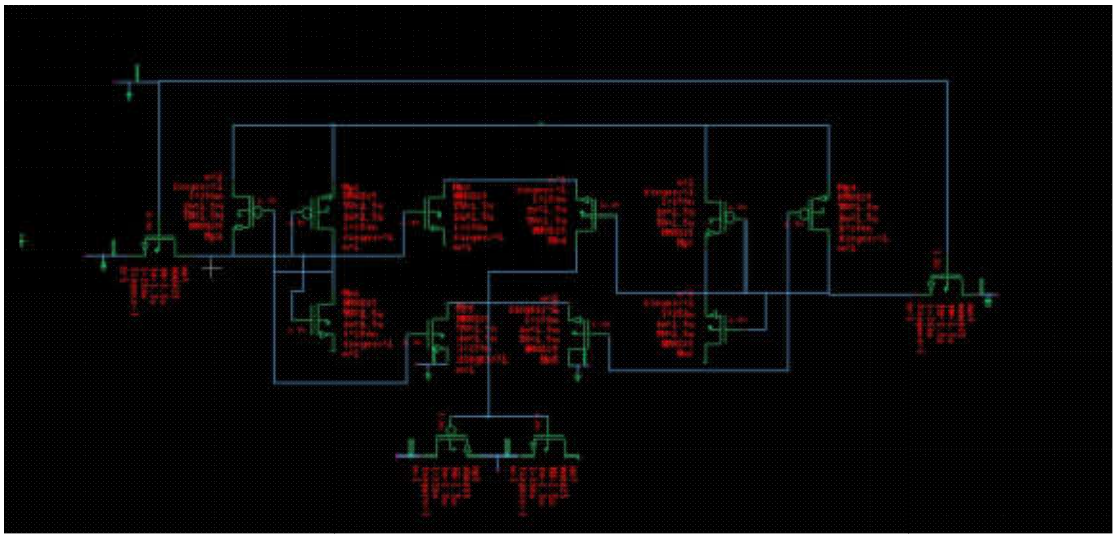


Fig 35 :Existing PF TCAM Cell

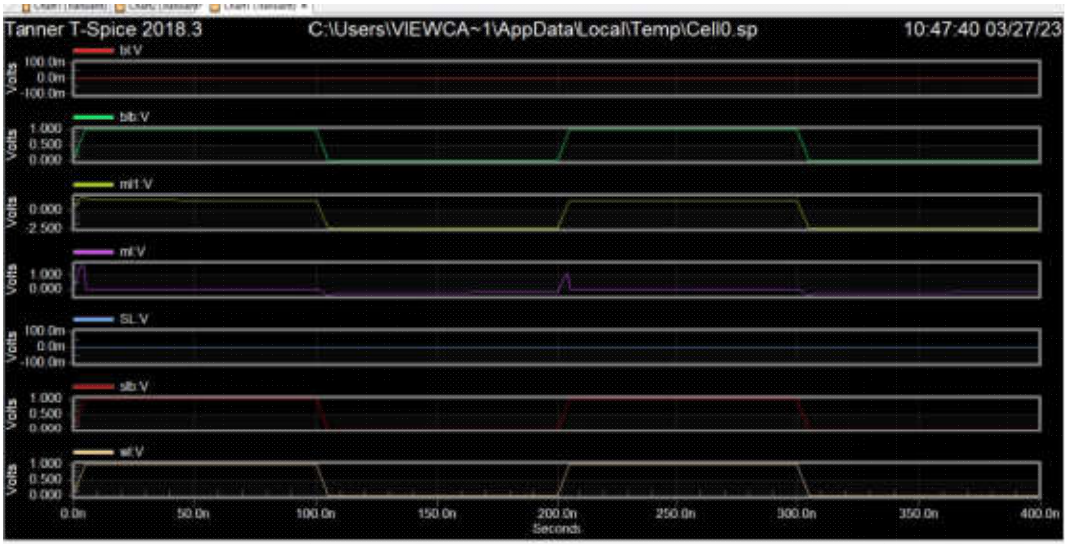


Fig : Simulated results of Existing PF TCAM Cell

The conventional TCAM and proposed TCAM were simulated for 1bits using tanner 45 nano meter technology. Simulated waveforms of conventional TCAM and proposed TCAM is presented respectively. With the help of the average power waveforms, it has been noticed that the average power consumption of conventional TCAM is 13.25nw and for proposed TCAM is 11.45nw.

The proposed 1bit TCAM is also simulated with the help of tanner and noticed that it takes 16% power reduction than the existed TCAM

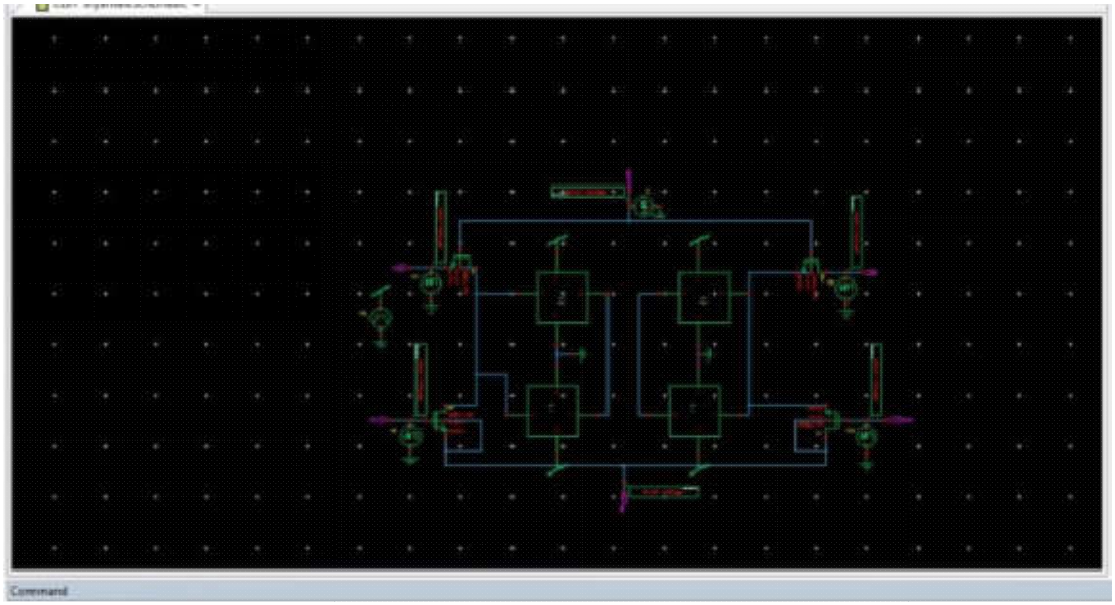


Fig 37 :Proposed PF TCAM Cell

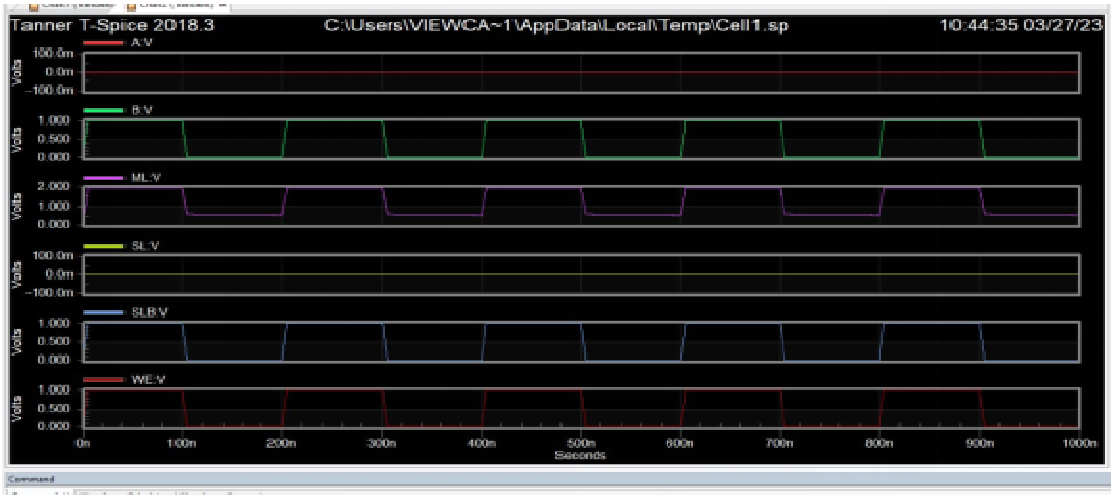


Fig 38 :Simulated Results for Proposed PF TCAM Cell

Performance parameters of the proposed PF-TCAM are analyzed through a random search vector of 16 bits on a 32*16-bit macro designed using tanner tool of 45nm CMOS technology

Parameters	Existing circuit	Proposed circuit
Power	13.45nw	11.25nw
Delay	0.1ns	0.29ns

Table : Comparison between Existing circuit and Proposed circuit

CONCLUSION:

This paper introduces a precharge-free searching approaching ternary CAM as an alternative solution to precharge type TCAMs. Absence of precharge cycle in the proposed precharge-free TCAM (PF-TCAM) reduces evaluation time by50%, which can enormously be useful in various applications involving search, association and computation. The introduced TCAM performs search in HALF clock cycle while existing TCAM designs .

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