Delay Optimization and Power Optimization of 4-Bit ALU Designed in FS-GDI Technique

KHANDAVILLI PRIYANKA[1]
M.Tech scholar
Department of Electronics and Communication Engineering
SWAMY VIVEKANANDA ENGINEERING COLLEGE, KALAVARAI, BOBBILI, VIZIANAGARAM
Andhra Pradesh, India.
Email – priyakandavilli31@gmail.com

BONTALAKOTI PRASAD KUMAR[2]
Assistant Professor M.Tech(PHD)
Department of Electronics and Communication Engineering
SWAMY VIVEKANANDA ENGINEERING COLLEGE, KALAVARAI, BOBBILI, VIZIANAGARAM,
Andhra Pradesh, India.
Email – prasad.ece.411@gmail.com

Abstract

In this paper we proposed a reduction of delay, leakage current, leakage power. First find out the leakage current and leakage power. Which uses a gate diffusion input technique. By using this no of transistor is reduced. If number of transistor is reduced, area is also reduced, leakage current also affected. To study all parameter in this thesis uses a 2x1 MUX, 4x1MUX,16x1 MUX and ALU. Applying a GDI technique and also implemented by using a CMOS technique. Then do comparisons on GDI and CMOS technique and do a capacitance calculation. To implement all those things use a microwind 3.1 and DSCH 2.0. It is an Electronic Design Automation (EDA) environment that allows implementing a integrating in a single framework different applications and tools, allowing supporting all the stages of IC design and verification from a single environment. The resulting layout must verify some geometric rules dependent on the technology (design rules). Now checked with a Design Rule Checker (DRC) to find any error in the layout diagram and them simulation is performed. In implementing and do a comparisons of GDI and CMOS technique

Keywords: - Reversible logic gates, Fredkin, Peres, Feynman, Toffoli, MAC, Array Multiplier and Ripple Carry Adder.

1. Introduction

One of the new research trends in recent years is reversible computing and designing of digital circuits and structures using reversible approach[1–3]. In modern digital architecture, the key feature of reversible logic is to reduce the power dissipation. Application areas therefore include but are not restricted to low-power CMOS architecture, quantum computing, thermodynamic technology, bio-info Modern digital systems and subsystems perform Tera-operations-per-second (TOPS), thus requiring rapid transfer of internal signals in terms of bit transitions (combination of 0s and 1s). We should note a few laws and con- ventions associated with the design of digital logic in this context. First, Moores law claimed that transistor numbers double approximately every two years. Second, the minimum possible amount of energy dissipated for each irreversible bit operation is approximately KT ln2 (in Joules), according to the Landauers theory. where Boltzmanns constant K = 1.38*10-23 (J/K) and T is the

absolute temperature of the computation [4, 5]. With technological advancement, the number of transistors can only increase day by day with reduced chip area causing increased dissipation of power as heat increases further. Even if the loss of one bit of information and the resulting heat dissipation, This sum seems negligible in the case of complex modern-day computations, and may reduce overall performance and also contribute to the ageing problem. According to[6] as long as the device is reversible by reproducing the inputs from its observed outputs, it would not dissipate the above-mentioned KT ln2 energy. The sum of energy dissipation is commensurate with the information loss in terms of bits lost during computation. Thus reversible logic gates can be used in modern high-speed power conscious circuits as basic building blocks. We can portray a reversible logic like black box (m m) with IV = ($I1$, $I2$, $I3$, ..., Im) as input vectors and OV = ($Q1$, $Q2$, $Q3$,, Qm) As output vectors as shown in Fig, respectively. 1. Thus, reversible logic is a one-to-one correspondence logic, where we can uniquely evaluate outputs from the given inputs and can quickly and uniquely reproduce inputs from the immediate outputs and go forward and backward at any computing point[5].

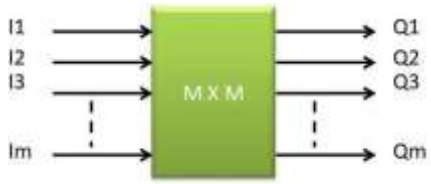

Fig. 1: General reversible logic block

This paper introduces a novel design method of low-cost, configurable RO PUF based on XOR Gate using reversible logic and Feynman gate logic only.

II Literature Survey

Here we present a comprehensive review of literature survey carried out on the high performance, small chip area and lower power consumption. The speed, the area, and the power consumption of the multiplier depend on the implementation of the PPG, the PPRT and the CPA. The PPG can be implemented either by using two input AND gate logic or the MBE scheme. The PPRT can be implemented either by using CSA tree structure or various types of compressors. The CPA can be implemented by using the CLA adder scheme, combining CLA and Carry Select scheme, CLA and Carry Skip scheme,MLCSMA, and by computing pre-sums logic. Hence, the literature review is carried out on the design and implementation of various types of the PPG, PPRT and CPA for the design and implementation of very high speed signed and unsigned multipliers. Since the performance of the multipliers can be enhanced by designing high speed PPG circuits many recent advanced papers [1, 2, 3, 4,], have been published. Since, the performance of the multipliers can also be enhanced to the most extent by designing high speed PPRT, many high performance papers [5, 9, 20], have been published. And finally since, the maximum speed of the multiplier depends on the performance of the Carry Propagate Adder (CPA), various high speed Carry Look-ahead(CLA) adder techniques [1, 10, 11], have been published. The present Modified Booth Encoding MBE [1, 2, 4, 6, 7] multiplier and the Baugh-Wooley multiplier [106] can perform multiplication operation on signed numbers and the array multiplier [6] can perform multiplication operation on unsigned numbers only. Thus, the

requirement of the modern computer system is a dedicated and very high speed unique multiplier unit for signed and unsigned numbers.

The high speed DSP and FFT computation requires high speed and dedicated multiplier units. Such high speed processors can perform parallel, pipeline, and superscalar pipelined operations. In order to improve the throughput of this type of system the processing stages are executed in parallel and pipeline techniques. In order to design the pipeline [34, 49, 53] multiplier with lesser number of the pipeline stages, smaller 4 × 4 or 8 × 8 array multiplier can be designed and used them in parallel to design large size multiplier, or it can be used to design superscalar pipeline multipliers for the matrix multiplication [5-13].For the high speed, low area, lower power consumption for array multiplier, MBEmultiplier, pipeline multiplier, inner product multiplier and matrix multiplier have been reviewed in the following section.

2.1 Review of Literature on High Performance Multiplier:

For the current states and future challenges the following papers have been reviewed in the literature survey.W. C. Yeh and C. W. Jen [1], have proposed a new Modified Booth Encoding (MBE)scheme as the Partial Product Generator (PPG). They have proposed the MBE using encoder and decoder logic. The delay path is optimized through encoder and decoder logic. They have also proposed Multiple-Level Conditional-Sum Adder (MLCSMA) as the Carry Propagate Adder (CPA) to improve the performance of the parallel multiplier. The parallel carry generator network of the MLCSMA provides carry in parallel to all the stages of the full adder. The proposed MBE algorithm and the MLCSMA algorithm can optimize the delay and finally reduces the delay by 8% compared with other parallel multipliers. This proposed multiplier can multiply signed number operands.

Shiann-RongKuang, Jiun-Ping Wang, and Cang-Yuan Guo [2], have proposed theMBE that generates regular partial product array. The MBE [1] uses extra partial product bit at the least significant bit (LSB) position of each partial product row and generates$\{(n/2) +1\}$ an irregular partial product array. The PPRT delay and the area increases due to extra bit needed for the negate operation. And therefore in [2] have proposed the MBE to generate a regular partial product array with $\{n/2\}$ partial product rows. Thus the reduction by one partial product row resulted in the reduction in the delay, the area, and the power of the MBE multipliers. But additional logic circuits have been implemented for converting irregular partial product to regular partial product extra logic circuits have been used. Since this uses regular MBE as the PPG and hence reported the higher performance compared to the conventional MBE multipliers.

Wang, Shyh–Jye Jou and Chung-Len Lee [3], have proposed a well-structured MBEmultiplier architecture. In this paper an improved Booth Encoder logic and Booth Selector logic have been proposed to remove an extra partial product row like paper [2]. This paper also proposed the design of spare-tree approach for two's complementation operation. Thus the removal of an extra partial product row and the design of sparse-tree approach resulted in the reduction of the area and improved in the speed of the signed multiplier.

G.Goto, A Inoue, R Ohe, S Kashiwakura, S Mitarai, T Tsuru, T Izawa [4], have proposed a 4.1 ns compact 54×54-bit multiplier utilizing sign-select Booth Encoders logic. To reduce the total transistor count, they have proposed the design of sign-select Booth encoding scheme. They have proposed also the design of 4-2 compressor using 48-transistors for the operation as the PPRT. The proposed sign-select Booth algorithm simplifies the Booth selector circuit such that the transistor count reduces by 45% as compared to the MBE scheme of [20, 21]. Thus, with the design of sign-select logic and 4-
2 compressor logic, for the design of 54 × 54-bit signed multiplier they have claimed the delay of multiplication is 4.1 ns, the chip area size is 1.04 mm × 1.27 mm at 2.5 V power supply, with reduction in total number of transistor by 24%.

C. H. Chang, J.G, and M. Zhang [5], have proposed the ultra-low-voltage and lowpower4–2 and 5–2 compressors implemented in CMOS logic for fast arithmetic circuits. They have proposed the design of 4-2 compressor using Exclusive OR (XOR) logic gates at three levels with the critical delay path of 3-units and the 5-2 compressor with critical delay path of 4-units. They also proposed that new circuit with a pair of

PMOS-NMOS transistors to eliminate the weak logic for the XOR and Exclusive NOR (XNOR) logic modules. They have claimed that the proposed XOR–XNOR module used for the implementation of 4-2and 5-2 compressors can operate at supply voltage as low as 0.6 V.

Huang, Ercegovac [6], have proposed the design of high-performance low-power left to array multiplier for signed number. They have proposed the signal flow optimization technique in the full-adder of the PPRT by using left-to-right leapfrog (LRLF) signal flow
and splitting the reduction array into upper/lower parts for high performance.

Pouya Asadi and KeivanNavi [7], have proposed the design of a Novel High-Speed54×54-bit multiplier for signed number. They have presented a self-timed carry-look ahead adder in which the average computation time was proportional to the logarithm of the logarithm of n. A novel 4-2 compressor using PTL has been developed and claimed speed over conventional CMOS circuits due to critical-path gate stages was minimized. The proposed multiplier delay was 3.4 ns at 1.3 V power supply and implemented the multiplier using 42579 transistors.

Leandro Z. Pieper, Eduardo A. C. da Costa, Sérgio J. M. de Almeida [8], have proposed 2's complement radix-2m array multiplier using dedicated modules. Using the dedicated modules 16, 32 and 64-bit multiplier have been implemented and claimed more
efficient to Modified Booth multiplier.

In [11], R. Zlatanovici, Sean Kao, Borivoje Nikolichave proposed a fast and energy-efficient single-cycle 64-bit CLA added. In this paper an optimized topology, a sparse radix-4 Ling adder and use of domino CMOS logic have beenclaimed the 240 ps delay for the addition 64-bit operands and fabricated in 90 nm CMOStechnology, consumes 260 m W at 1 V power supply.

In [14], A M. Shams, Tarek K. D, Magdy A. Bayoumi have proposed the design and implementation of Low-Power 1-bit CMOS full adder cell. They have been proposed 20different 1-bit full adder cells. Each full adder cells have been the different value of the delay, the area and the power consumption. From the library of the full adder cells the designer of the circuit can pick an appropriate adder that meet the requirement.

In [18], Kiwon Choi and Minkyu Song have proposed a high performance multiplier for a DSP using a novel sign select Booth encoder and a novel compound full-adder. For the multiplication of 32 × 32-bit signed number a 64-bit conditional sum adder has been proposed. From the experimental results, various parameters measured have been the delay of 9.8 ns and power consumption of 186 mW at 100 MHz at 3.3 V power supply.

In [19], A Nève, H Schettler, T Ludwig, D Flandre have proposed a 64-bit carry-select adder high performance and low-power dissipation. The delay power product has be entreated as the figure of merit for the high speed and lower power consumption. The global carry network (GCN) and the selection of 8-bit pre-sums, the 64-bit adder with 23 empower dissipation and the delay of 326 ps. V Oklobdzija, D Vileger, Simon S. Liu [22], have proposed an algorithm for generation of a high speed parallel multiplier. It uses the minimal number of cells in the PPRT for the delay optimization. Simulation results have been tested in l ps CMOS ASIC technology.

III EXISTING SYSTEM

- designing high speed PPG circuits many existing system have been implemented Since, the performance of the multipliers can also be enhanced to the most extent by designing high speed PPRT

- Carry Propagate Adder (CPA), various high speed Carry Look- ahead (CLA) adder techniques have been used in Existing system

As we pack more and more logic elements into smaller and smaller volumes and clock them at higher and higher frequencies, we dissipate more and more heat. This creates at least three problems:

- Energy costs money.
- Portable systems exhaust their batteries.
- Systems overheat

When a computational system erases a bit of information, it must dissipate **ln 2 x *kT* energy**, where *k* is Boltzmann's constant and *T* is the temperature. For *T* = 300 Kelvins (room temperature), this is about 2.9 x 10^-21 joules. This is roughly the kinetic energy of a single air molecule at room temperature. Today's computers erase a bit of information (in the sense used here) every time they perform a logic operation. These logic operations are therefore called "irreversible." This erasure is done very inefficiently, and much more than *kT* is dissipated for each bit erased. If we are to continue the revolution in computer hardware performance we must continue to reduce the energy dissipated by each logic operation. Today, because we are dissipating much more than *kT*, we can do this by improving conventional methods, i.e., by improving the efficiency with which we erase information. An alternative is to use logic operations that do not erase information. These are called *reversible* logic operations, and in principle they can dissipate arbitrarily little heat. As the energy dissipated per Irreversible logic operation approaches the fundamental limit of ln 2 x *kT*, the use of reversible operations is likely to become more attractive. If current trends continue this should occur sometime in the 2010 to 2020 timeframe. If we are to reduce energy dissipation per logic operation below ln 2 x *kT* we will be *forced* to use reversible logic.

3.1 RELATION WITH THERMODYNAMICS:

As was first argued by Rolf Landauer of IBM, in order for a computational process to be physically reversible, it must also be *logically reversible*. Landauer's principle is the rigorously valid observation that the oblivious erasure of *n* bits of known information must always incur a cost of *nkT* ln(2) in thermodynamic entropy. A discrete, deterministic computational process is said to be logically reversible if the transition function that maps old computational states to new ones is a one-to-one function; i.e. the output logical states uniquely defines the input logical states of the computational operation.

3.2 PHYSICAL REVERSIBILITY

The implementation of reversible computing thus amounts to learning how to characterize and control the physical dynamics of mechanisms to carry out desired computational operations so precisely that we can accumulate a negligible total amount of uncertainty regarding the complete physical state of the mechanism, per each logic operation that is performed. In other words, we would need to precisely track the state

of the active energy that is involved in carrying out computational operations within the machine, and design the machine in such a way that the majority of this energy is recovered in an organized form that can be reused for subsequent operations, rather than being permitted to dissipate into the form of heat.

3.3 LOGICAL REVERSIBILITY

To implement reversible computation, estimate its cost, and to judge its limits, it can be formalized in terms of gate-level circuits. A simplified model of such circuits is one in which inputs are consumed (however, note that real logic gates as implemented e.g. in CMOS do not do this). In this modeling framework, an inverter (logic gate) (NOT) gate is reversible because it can be *undone*. The exclusive or (XOR) gate is irreversible because its two inputs cannot be unambiguously reconstructed from its single output. However, a reversible version of the XOR gate—the controlled NOT gate (CNOT)—can be defined

by preserving one of the inputs. The three-input variant of the CNOT gate is called the Toffoli gate. It preserves two of its inputs *a,b* and replaces the third *c* by With this gives the AND function, and with this gives the NOT function. Thus, the Toffoli gate is universal and can implement any reversible Boolean function (given enough zero-initialized ancillary bits). More generally, reversible gates that consume their input have no more inputs than outputs. A reversible circuit connects reversible gates without fanouts and loops. Therefore, such circuits contain equal numbers of input and output wires, each going through an entire circuit. Similarly, in the Turing machine model of computation, a reversible Turing machine is one whose transition function is invertible, so that each machine state has at most one predecessor.

3.4 VARIOUS REVERSIBLE LOGICS:

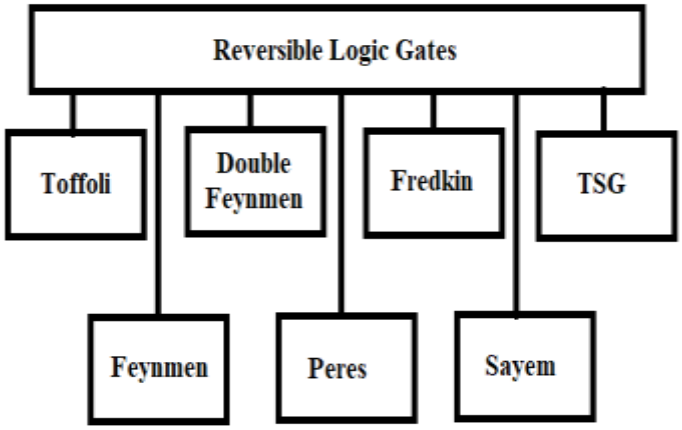

Fig. 2 Reversible Logic gates

The above Figure represent the different types Logics are available in Reversible gates.

IV. Proposed system

For the objective of get rid of undesirable equipment during handling the 4-Bit Reversible multiplier unit and 8-Bit Reversible snake and 8-Bit Reversible gatherer are utilized in the proposed MAC design.This improves the speed of operation of the MAC and also reduces the area.

4-Bit Multiplier unit operation describes below**.**

Multiplicand:

S3 S2 S1 S0

Multiplier:

J3 J2 J1 J0

R Q P O N M L K

Product:

PP7 PP6 PP5 PP4 PP3 PP2 PP1 PP0

Main purpose of using reversible multiplier instead of conventional multiplier is, this we notice a reduction in computations, basing on reduction of total number of operations. This factor gives proposed MAC unit design extra efficient compared to the existing one.in the proposed architecture by using limited hardware is established for only low power dissipation and fast operation.

A. 4 Bit Array Multiplier:

Below figure shows the 4 x 4 Bit array multiplier. Basic working principal is depends on the rule of shift and algorithm. By using AND gates the partial products can be produced and their summation can be performed by utilizing Full and Half Adders. All the operation in the n x n array multiplier are performed by utilizing Half Adders and n x (n-2) Full Adders. The bit array is designed by using the pipelined structure. Delay of the bit array multiplier equal to the width of the multiplier and speed of response will be reduced for wide fan-in multipliers.

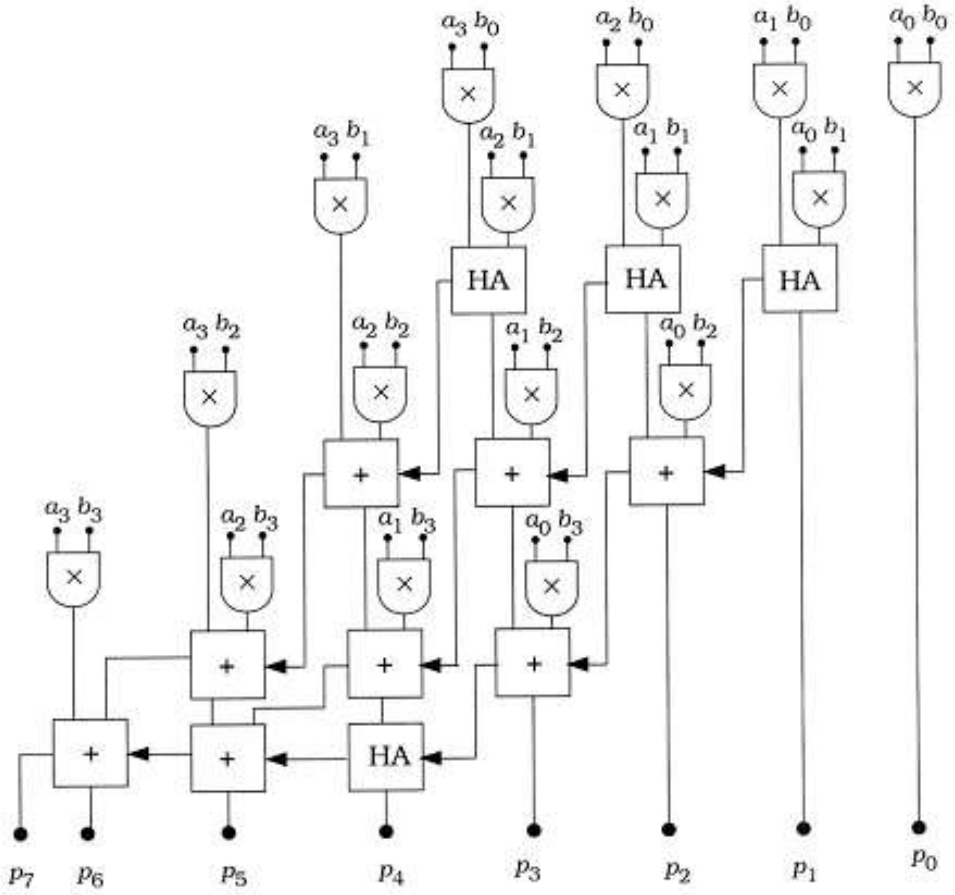

Fig 3: An 8 × 8-bit unsigned array multiplier

Figure 3 shows the generation of 4 partial products for 4 × 4-bit unsigned array multiplier. This uses two input AND gate logic for producing each partial product bit. Figure 4.2 shows the structure of each cell (C) of array multiplier, which function as the partial product generator and full adder (PPGA). Figure 4.3 shows the architecture of an array multiplier that requires 16 cells of Figure 3 to produce an 8-bit product.

a3 a2 a1 a0
× b3 b2 b1 b0

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a3b0 a2b0 a1b0 a0b0 PP1

a3b1 a2b1 a1b1 a0b1 PP2
a3b2 a2b2 a1b2 a0b2 PP3
a3b3 a2b3 a1b3 a0b3 PP4

p7 p6 p5 p4 p3 p2 p1 p0

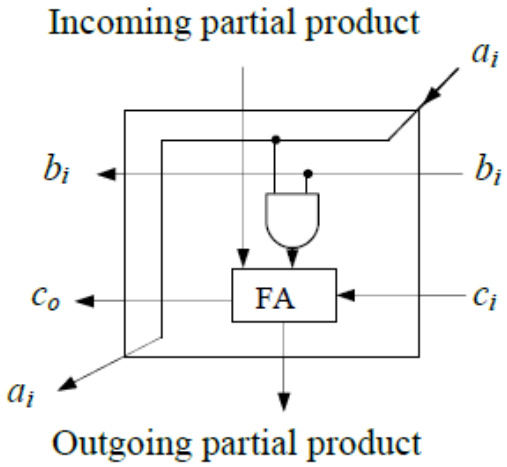

Fig 4: PPGA Cell (C)

Below figure shows the 4 x 4 Bit array multiplier. Basic working principal is depends on the rule of shift and algorithm. By using AND gates the partial products can be produced and their summation can be performed by utilizing Full and Half Adders. All the operation in the n x n array multiplier are performed by utilizing Half Adders and n x (n-2) Full Adders. The bit array is designed by using the pipelined structure. Delay of the bit array multiplier equal to the width of the multiplier and speed of response will be reduced for wide fan-in multipliers.

B. 8-Bit Ripple Carry Adder :

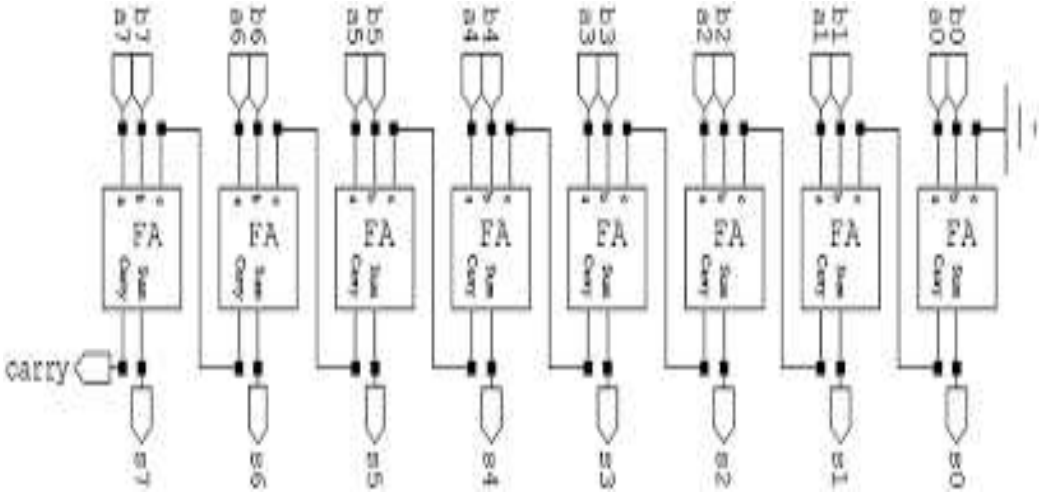

Fig 5. 8-Bit Ripple Carry adder

A Full adder describes that takes two input bits, a carry-in bit and produces the output sum and carry out. One type of reversible full adder is discussed and it is implemented with Peres gate. The 3x3 Peres Gate is singly worked as half adder circuit when third input is set to zero i.e. third input is treated as a constant input. To implement the Reversible full adder circuit using Peres gate it requires two Peres gates which should be arranged as shown in Fig 6. Now this entire circuit is denoted as name Peres Full Adder Gate (PFAG). Peres logic Full Adder Gate produces two garbage outputs (SJ1 and SJ2), and requires one constant input. The constant input is set to zero to obtain the desire outputs.

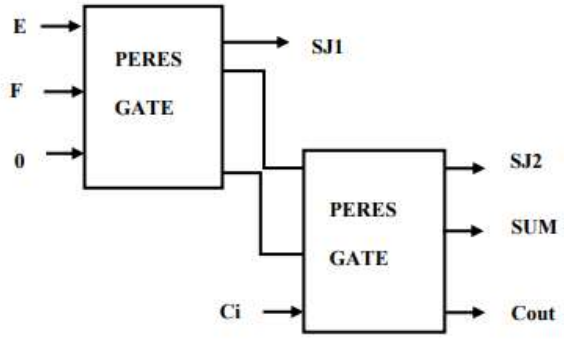

Fig 6 :-Peres Gates Reversible full adder

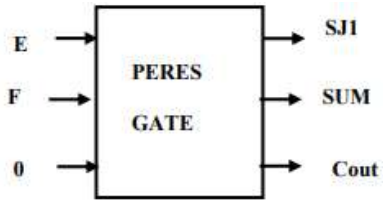

Fig 7:- Peres Gates as Reversible Half adder

V . EVALUATED RESULTS

The proposed PUF is based on Feynman gate (FG), which is a logic gate which is reversible. FG is a reversible 2X2 dimensional logic gate. FG has two outputs; one is a copy from an input ('garbage') and the other is the product of XOR from the two inputs. FG is therefore used as a copy gate, it is therefore useful for duplicating the necessary outputs The simulation Results discussed MAC design by using 4X4 Array Multiplier in reversible logic gate like Peres gate are modelled using VHDL module. The practical verification is done and synthesized in Xilinx ISE.

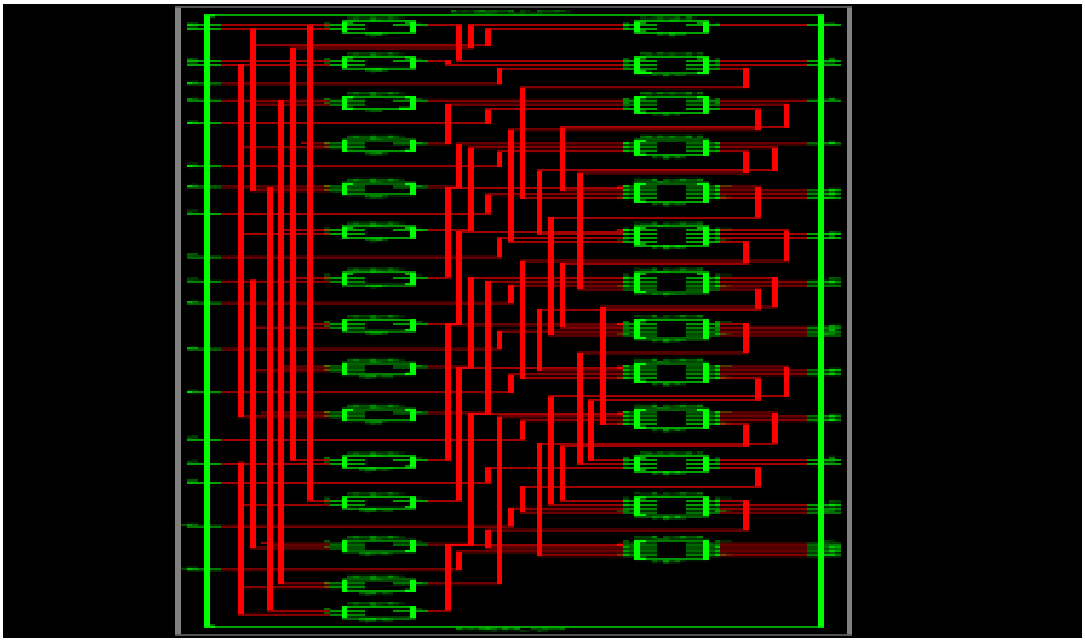

Fig. 8. RTL Schematic of 4 Bit Array Multiplier

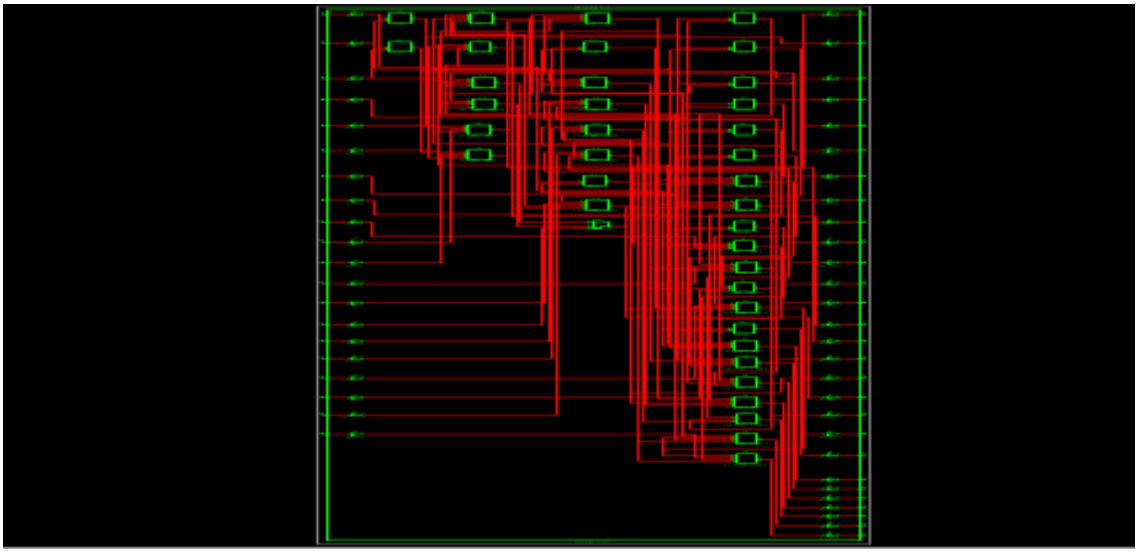

Fig. 9. Technology View of 4 Bit Array Multiplier

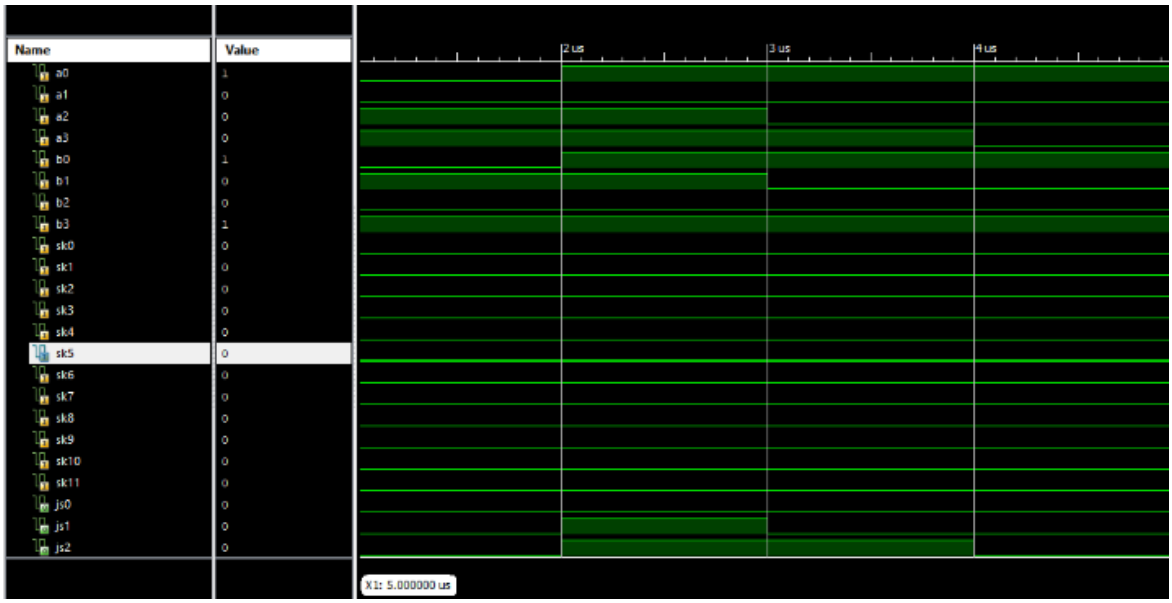

Fig. 10. Output Waveform of 4 Bit Array Multiplier

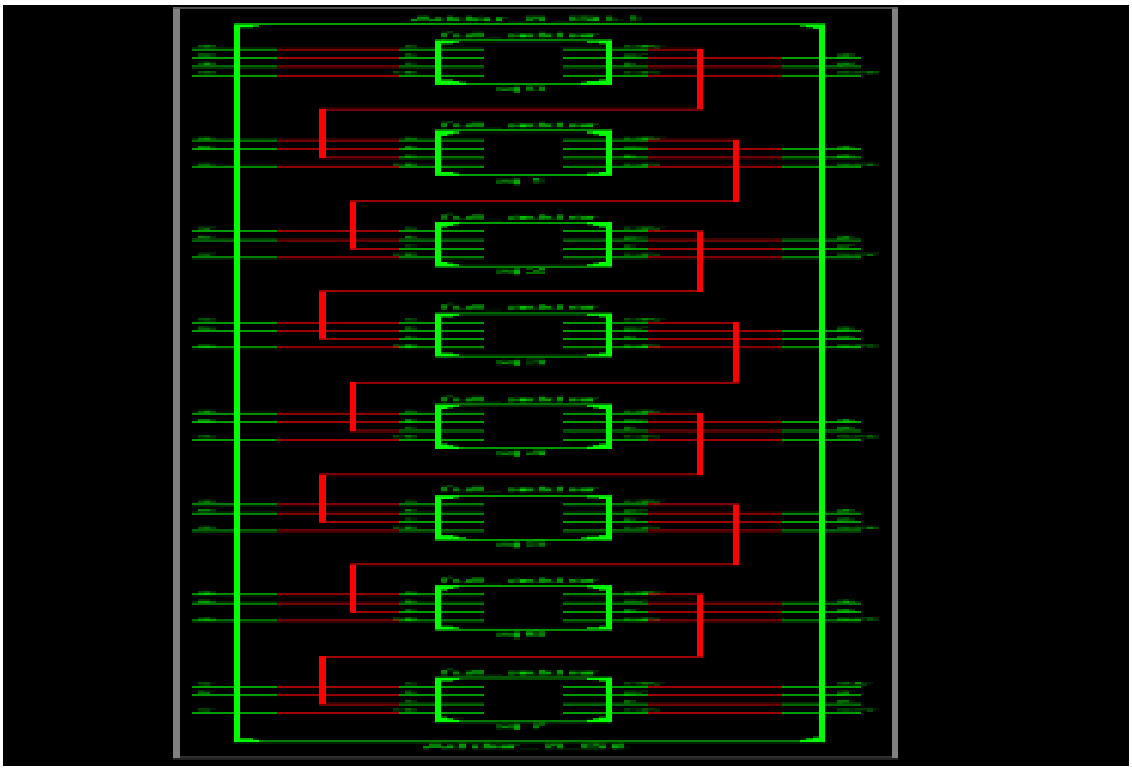

Fig. 11. RTL Schematic of 8-Bit Ripple Carry Adder

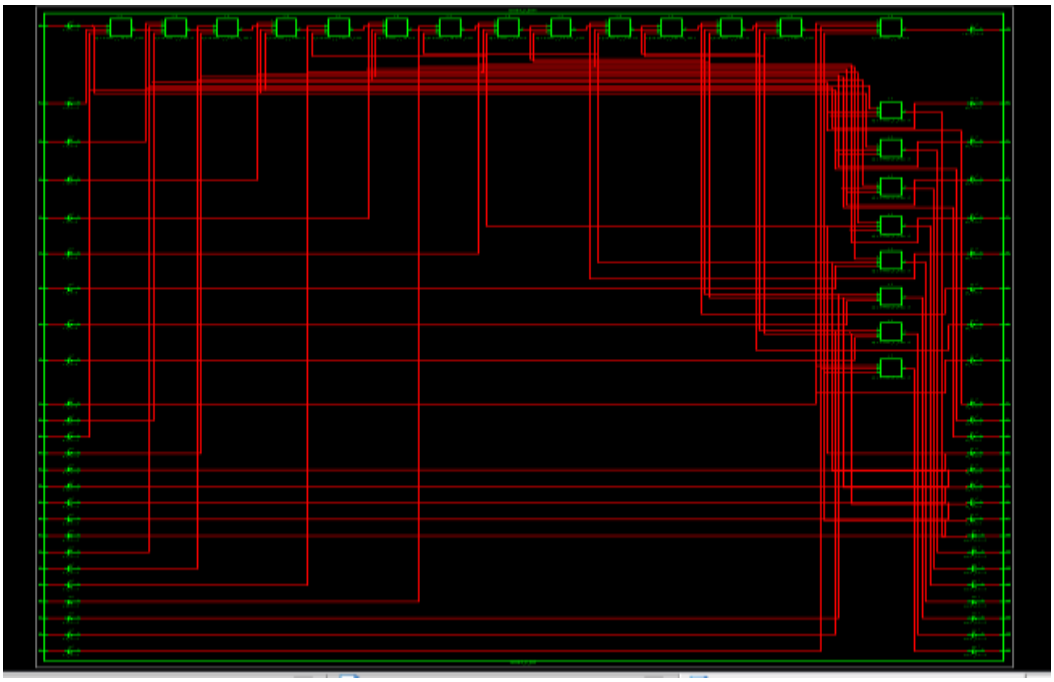

Fig. 12 Technology View of 8-Bit Ripple Carry Adder

Fig. 13. Output Waveform of 8-Bit Ripple Carry Adder

Peres Gate based MAC	No.of Slices	No.of LUT's	No.of Bounded I/O's	Delay
4X4 Array Multiplier	21	37	48	16.52ns
8-Bit Ripple Carry adder	13	22	50	24.48ns
4-Bit MAC	25	42	22	32.64ns

Table 1:- PROPAGATION DELAY AND AREA COMPARISON

VI. Conclusion And Future Scope

4-Bit MAC design in Reversible Logic based on the Peres Logic. The performance of 4-Bit Array Multiplier can be improved using reversible logic and evaluate the number of gate count, garbage output, quantum cost and delay of the 4-Bit Array Multiplier implemented using Reversible logic operation by using Peres Gate.

FUTURE SCOPE:

Future research may require but is not limited to the following
i. Further reduction in the in the size of PPG, PPRT and CPA is possible by usingtransmission gate logic, which can result into the area efficient and lower powerconsumption multiplier. Use of transmission gate (CMOS switch) really decreasesthe number of transistors and buffers are not needed as they produce strong logic-1and strong logic-0 outputs. But the use of transmission gate more in series maycause more delay, therefore careful design of the circuit architecture is needed.
ii. All the hardware implemented in this dissertation can be extended to the fixed pointand floating point number system. The NMBE and MMBE PPG circuits can beused to generate the partial products. In fixed point for the precision multiplicationoperation, it is necessary to allocate more number of bits. For the floating pointnumber IEEE single precision 32-bit and double precision 64-bit formats areavailable.
iii. Synthesis process is carried out for PPG, PPRT and CPA separately. For simplicitywiring capacitances and load capacitances are not extracted. Synthesizing the wholemultiplier circuit and considering effects of wiring and load capacitances the realintegrated circuit multiplier can be designed.
iv. By further splitting the pipeline stages up to seven, the pipeline multiplier can beoperated with 30 GHz synchronous clock signal. Since the delay of the NMBE orMMBE is very small and the CLCSA takes maximum delay and VCA even closerto the CLCSA, therefore dividing the CLCSA and VCA stages the pipeline clocksignal frequency can be increased to about 30GHz.

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