EFFICIENT 32-BIT BCD ADDER USING QUANTUM DOT CELLULAR AUTOMATA

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Abstract--- In the current era of technology the size of the system needs to be reduced in order to make compact as well as portable simultaneously it must process the data at very high speed with less delay. To design such circuits, we need new approach to stand with such requirements.

In this paper we will present emerging technique of designing which is termed as Quantum-dot Cellular Automata (QCA).

QCA is the technology where the significant improvement is possible in order to design more complicated circuits. Here we are suggesting a new approach to design QCA-based 32 bits BCD adder.
Keywords- BCD adders, decimal arithmetic, Quantum Computing, Low Power, majority gates (MG), quantum-dot cellular automata (QCA).

I. INTRODUCITON

Continued and fast dimensional scaling of CMOS eventually will approach the fundamental limit. Also, Short channel effects, high power dissipation, quantum effects are limiting the further scaling of current CMOS technology devices [2-3]. Emerging device technology can overcome the scaling limitation in the current CMOS technology. Single Electron Transistor (SET), Quantum-dot Cellular Automata (QCA) and Resonant Tunneling Diodes (RTD) are some of the "Beyond CMOS" technologies. Among these evolving nanotechnologies, Quantum-dot Cellular Automata is the most favorable technology. QCA is transistor less computational paradigm which can achieve device density of 1012 devices/cm2 and operating speed of THz. QCA device paradigm replaces FET based logic and exploit the quantum effects of small size. Quantum-dot Cellular Automata is a mean of representing binary information on cells, through which no current flows, and achieving device performance by the coupling of those cells

This Paper is Organized as follows Section II will gives you the details of the software used to prepare this project, Section III deals with the Structure of QCA cell and its polarization and QCA background Section IV gives you the design and implementation efficient 32-bit BCD adder, Section V deals with the outcome of the project and finally Section VI gives the Conclusion and Future Scope & some of the references of this project.

II.SOFTWAREUSED

QCA designer is the product of an ongoing effect to create a rapid and accurate simulation and layout tool. for quantum-dot cellular automata (QCA). It is capable of simulating complex QCA circuits on most standard platforms. And it is an ongoing research effect by the Walus Lab at the University of British Coloumbia to create a design and simulation tool for QCA. This tool is still under development and is provided free of cost to the research community "as is". QCA is an emerging concept in computational nanotechnology for the realization of computer using arrays of nano-scale QCA cells. These QCA cells are capable of performing all complex computational functions required for general-purpose computation (majority function, Inversion, and fan-out). The QCADesigner tool facilitates rapid design, layout and simulation of QCA circuits by providing powerful CAD features available in more complex circuit design tools.

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III. STRUCTURE OF QCA CELL AND POLARIZATION

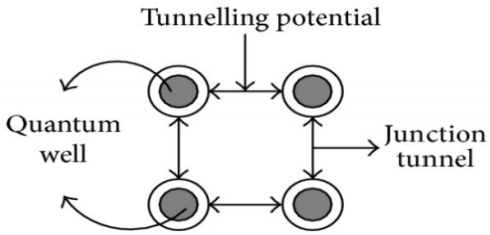
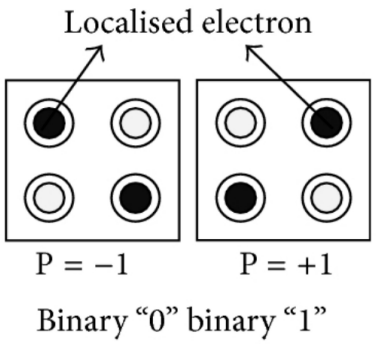


Fig. 1 Structure of a QCA Cell

The most fundamental element of the QCA structure is shown in figure 1. It is the building block of the QCA technology. As we can see in the figure it is having four dots at all its corner. The structure has two free electrons. The structure of the QCA in provided in
the figure 1.



Because of the coulombic repulsion these two electrons can only be placed in two stable states. The electrons are always resided in diagonally opposite corners of the QCA cell. The diagonally opposite corners are having maximum distance. The stable states also called as polarization. As per the locations of the electrons in the cell two states can be take place. These states are considered as
binary states 1 and 0. For the purpose of explanation the figure 2 is shown.

The diagonally opposite electrons interact to each other by the electrostatic forces and due to this force the electrons maintain its polarization. However the QCA cells cannot flow the data intrinsically therefore to get the control over flow of the direction of electrons the four clock zones are associated. These four clock signal have 90◦
phase difference. The QCA design is partitioned into clock zones. The clock scheme, named the zone clocking scheme, makes the QCA designs different polarizations intrinsically
pipelined.

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IV. 32 BIT BCD ADDER

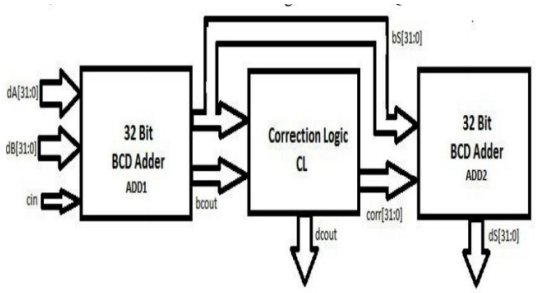


Fig 3.Structure of the 32 bits BCD adder.

In brief this proposes a unique approach to develop a QCA- based 32 bits BCD adder which can achieve higher computational speed than existing counterparts with occupying less area or count cell. The novel 1-digit decimal adder generates, propagates, and absorbs
a carry signal with delay times up to 27%, 45%, and 44% lower than the faster existing counterparts that are those described in differently from all previous works, we extended our work to the design of a 32-bits QCA-based BCD adder.

The BCD adder here presented follows the traditional top-level structure illustrated in Fig. 3, but it exploits the novel logic expressions demonstrated in the following by Equations1 and 2.

As the main result, the proposed approach leads to the best trade off between the overall occupied area and the speed performances.
To understand the new design strategy, let us examine first the 4 bits binary adder ADD1. 4 bit binary adder ADD1 collects the value of input dA(3:0) and dB(3:0) as well as its carry “cin” and figure out its binary output as bS(3:0) and “bcout”, this whole process it carried out as per the equation (2a) that introduces only one Majority gate(MG) between Ci and Ci+1.

Generally BCD means Binary Coded Decimal as we know decimal values means 0-9 so that if the output of the BCD adder result is greater than 9 or when the carry is "1" then we Add 6 to the obtained output to get the valid BCD Value. The reason for to add 6 to the UNBCD output is the in hexadecimal the difference between the maximum value and to the 9 is 6.
And this 32 bit BCD adder consists of 2 32bit binary adders and correction logic which consists of AND & OR gates .

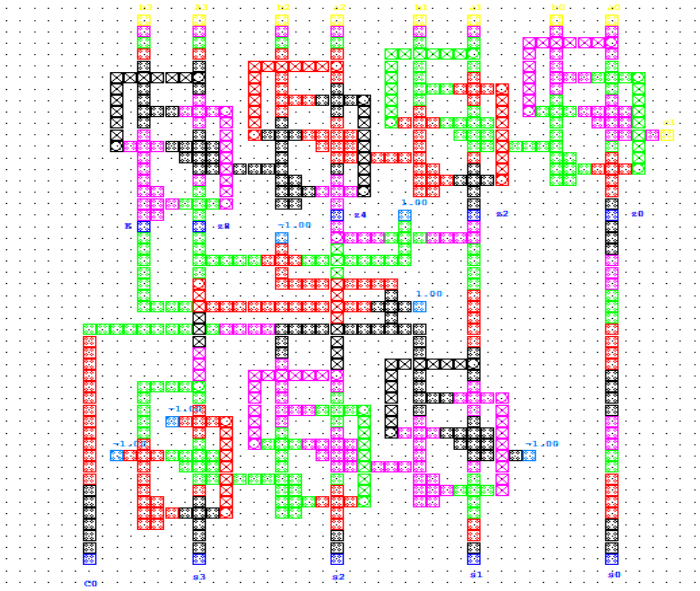


Fig 1 digit BCD adder in QCA.

V. OUTPUT

As the Simulation figure shows the output of the developed BCD adder The total number of inputs are three in which “a” and “b” are inputs whereas the third input is carry-in. It carries the value which was generated during the last operation. If there is no carry then put zero as its value. There are two outputs in the whole system. The first output is Sum which is represented by “sum”. The size of “s” is 32bits. Another output is carryout and its represented as “cout” The “cout” having the capability of holding 1 bit value.

Inputs

a[31:0]= 32'b00000000000000000000000000001000,

b[31:0]= 32'b00000000000000000000000000000100,

cin=0;

Outputs

s[31:0] = 32'b00000000000000000000000010010,

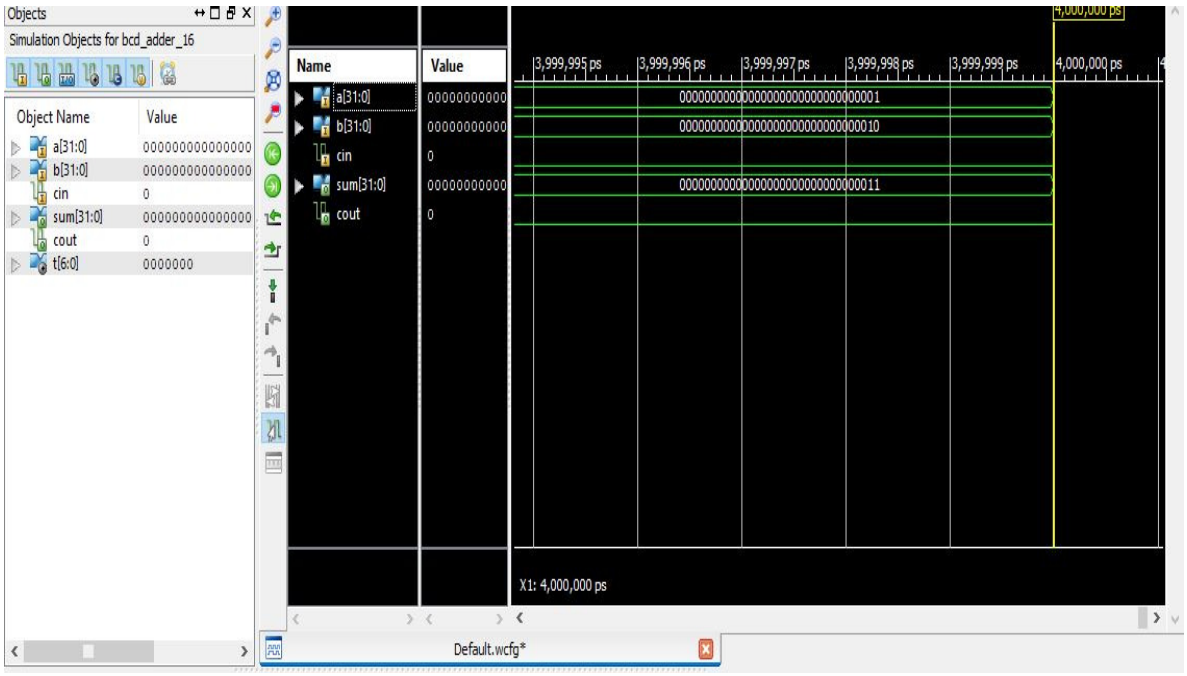
cout=0,

So here the QCA implementation shows that we need4 full adder at the top of the block for adding two 4bit binary numbers and there is a correction logic which consists of AND& OR gates.

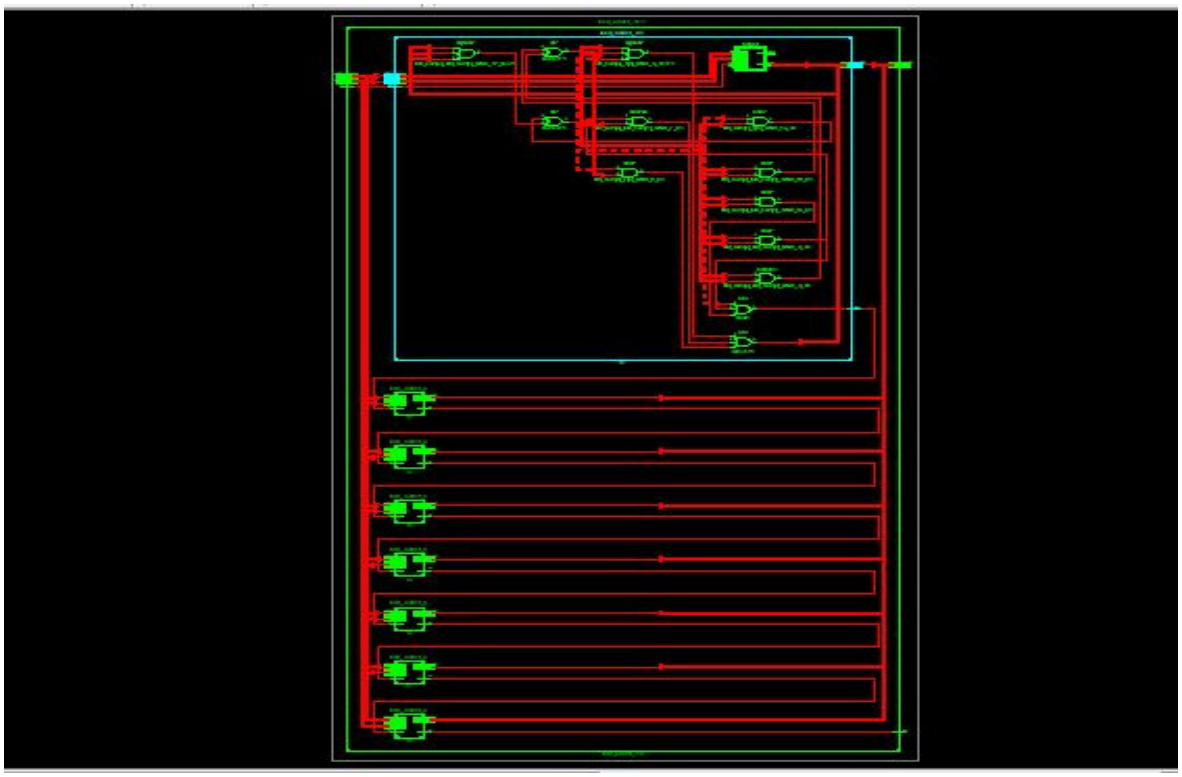
And we need 3 Full Adders at the bottom to add 6 0r 0 to the output of the first 4 full adders.

Generally we developed 1 digit BCD adder in QCA due to circuit complexity and increase in the complexity of the ouput we developed the 32 bit BCD adder in Xlinx and we observed the simulation waveforms and the RTL schematic in Xilinx.

SIMULATION WAVEFORM



RTL SCHEMATIC



The figure shows the RTL schematic of the 32 bit BCD adder In this we have first developed an VHDL code for the 4 bit BCD adder then with the help of this 4 bit BCD adder we have developed 32 bit BCD adder

Here we have used Eight 4 bit BCD adders the output of one 1 digit BCD adder is added as the Carryin to next 1 digit BCD adder and at last the output of the 8th BCD adder is taken as cout.

VI .CONCLUSION

The proposed work is focused on to develop a 32 bit BCD adder by adding two 32 bit BCD adder using Binary adders and if the sum is not valid BCD then we add 6 to the sum to get the valid BCD value. So by using this we have developed the Simulation Waveforms and RTL Schematic of BCD adder.

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