AN EFFICIENT DESIGN OF 16 BIT MAC UNIT USING VEDIC MATHEMATICS

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ABSTRACT

Vedic Mathematics is the old methodology of Indian mathematics which as has an intriguing technique for figuring's reliant on 16 conditions these are gotten from "Vedas". Multiplier is the fundamental piece of Digital Signal Processors (DSP's). By temperance of those made in one phase which diminishes the carry utilization of the Vedic mathematics and their application to the stunning multiplier ensure liberal decline of proliferation delay in assessment with DA based architecture and equivalent adder-based execution which is most commonly used architectures. The convenience of these circuits was checked and execution of limits like proliferation postponement and dynamic power use was controlled by Xilinx ISE Design Tool 14.7. This paper proposes the design of high-speed Vedic Multiplier using the methodology of Vedic Mathematics that have been modified to improve execution using Carry save adders. A high-speed processor depends altogether upon the multiplier as it is one of the key hardware blocks in most digital signal taking care of systems similarly as all things considered processors. This paper shows the architecture for a 16×16 Vedic multiplier module using Urdhva Tiryagbhyam Sutra. The paper by then loosens up increment to 16×16 Vedic multiplier using "Nikhilam Sutra" system. Further, the Verilog HDL coding of Urdhva tiryakbhyam Sutra and Nikhilam Sutra for 16x16 pieces duplication and carry save adder is imitated and executed on Xilinx ISE 14.7.

I. INTRODUCTION

Vedic mathematics was rediscovered in the mid-20th century from old Indian models (Vedas). Old Indian arrangement of mathematics was gotten from Vedic Sutras. The ordinary numerical calculations can be rearranged and even streamlined by the utilization of Vedic mathematics. The Vedic calculations can be applied to math, geometry, plain and round calculation, analytics. In [1], creators have proposed another multiplier dependent on a Vedic calculation for low force and fast applications. Their multiplier architecture depends on creating every incomplete item and their wholes in a single step. They guarantee that their proposed Vedic multiplier is quicker than the comparing exhibit multiplier and Booth multiplier. The creators in [2] have tried and analyzed different multiplier executions, for example, Array multiplier, Multiplier large scale, Vedic multiplier with full parceling, Vedic multiplier utilizing 4 cycle full scale, completely Recursive Vedic multiplier, Vedic multiplier utilizing 8 digit large scale for ideal speed. They have guaranteed that Vedic technique isn't on a very basic level not the same as customary strategy for augmentation. The execution of Rivest, Shamir and Adleman (RSA) encryption/unscrambling calculation utilizing Vedic mathematics is proposed to improve execution in [3]. They have utilized Vedic multiplier and division architecture in the RSA hardware for improved proficiency. Their outcomes show that RSA hardware actualized utilizing Vedic division and augmentation is productive as far as region/speed contrasted with its usage utilizing traditional duplication and division architectures. Dhillon and Mitra [4] proposed a multiplier utilizing "Urdhva Tiryagbhyam" calculation, which is advanced by "Nikhilam" calculation. They have recommended a decreased piece augmentation calculation utilizing "Urdhva Tiryakbhyam" and "Nikhilam" Sutra. We have built up another Vedic multiplier structure utilizing "Nikhilam" Sutra. The carry save viper executed in the proposed architecture diminishes propagation delay altogether. It is accepted that our architecture may set new way for future exploration.

II. LITERATURE REVIEW

Any spot there is a necessity for predominant handling applications there is an away from of a powerful quick multiplier. Enlargement takes most colossal time when appeared differently in relation to other number shuffling undertakings. Multipliers are the most basic squares in predominant enrolling architecture like Digital signal getting ready (DSP). Mac unit which include Multiplier and Accumulator expects a critical part to pick the introduction of any DSP block. The better introduction of MAC unit fulfills the limit of fast figuring and consistent dealing with capacities of a DSP. All through the drawn-out number of considerations has been proposed to improve the introduction and diminish the extraordinary partial thing term age during standard increase approach. In this paper, we have focused in on proposing the MAC architecture using a fused Hybrid twofold Multiplier and facilitated CLA adder association. The consolidated multiplier is a mix of Karatsuba computation and Urdhva Triyagbhyam sutra from vedic mathematics. CLA adder network involve CLA and prohibitive total adder which helps with diminishing extension time by performing equivalent development. Referred to design is executed in Verilog HDL using Libero SOC PolarFire v2.1 apparatus, zeroing in on its PolarFire FPGA family and MPF300T_ES-1FCG484E device.

A gainful equivalent multiplier and gatherer (MAC) unit subject to Vedic mathematics is presented. Vedic mathematics utilizes the Urdhva-

tiryagbhyam sutra for the multiplier design. The proposed MAC architecture redesigns the speed of movement while reducing the doorway district and power dispersing. We similarly achieve improved deferral with the help of Vedic encoder followed by the departure of finder stage by parallelizing the moderate results dealing with the data. Such pipelining of the midway results, before the last adder, has the effect of joining the aggregator stage with the partial thing period of the multiplier. Further, the overall computation speed of MAC unit is raised by the successful use of higher solicitation blowers in the combined fragmentary thing pressing factor and authority (PPCA) architecture. The area, timing and power reports show that, the essential path postponement of the proposed design is through and through decreased and it beats the current designs. We report a level out advancement of 20-30% and 7-18% independently for the 4-cycle and 8-digit Vedic MAC units, with respect to its full-scale circuit power, essential way deferral and cell domain. The architecture was coordinated using standard 90nm CMOS library and completed on Altera's Cyclone II course of action FPGA.

Growth is key limit in number shuffling exercises. Increase based exercises, for instance, copy and Accumulate unit (MAC), convolution, Fast Fourier Transform (FFT), isolating is by and large used in signal taking care of utilizations. As, duplication controls the execution period of DSP structures, there is need to develop quick multipliers. Old Vedic mathematics supports the response for some degree. In this paper, thought of Urdhva-Tiryagbhyam is used i.e., vertically and transversely duplication to execute 16×16 Bit Vedic multiplier and progression is cultivated by using carry save adders. Differentiating and past architectures, proposed architecture achieves 33.26% diminishing in combinational way delay. The Vedic multiplier proposed is completed in VHDL while fused and reenacted using Xilinx ISE Design Suite 14.5.

In VLSI Design, low power decline is refined by generally lessening the power. As of now, low power designs are pervasive in VLSI due to various reasons. The rule place is to diminish the glow in the device. From the central mathematical states of power, decline of power ought to be conceivable by either lessening clock, decreasing voltage or reducing trouble. The option of decreasing power ought to be conceivable by reducing voltage as clock should be kept up for speedier structures. Power decline ought to be conceivable at various levels like architecture, reasoning and semiconductor. Lessening of power and zone ought to be conceivable by relinquishing one factor to achieve the other. In this work, a corner multiplier is designed reliant on probabilistic technique. In the truncation part of partial things, a probabilistic evaluation inclination circuit is introduced. Wave Carry Adder (RCA) was superseded with Carry Look Ahead (CLA) adder in the use. Amusements were finished using Synopsys Design Compiler for saed 90nm development. 9.7% area decline and 3.9%power abatement was represented L=8 and L=10 when differentiated and existing work.

An Artificial neural association (ANN) is equivalent Information planning structure involves dealing with units. The planning unit picks while the association is compelling or not. So to design a capable planning unit and it moreover give better execution. The getting ready unit involves MAC unit (Multiplication and Accumulation) and Activation unit. In a current system, the getting ready MAC unit was designed by Booth multiplier and carry look forward adder. The current getting ready unit gives postponement and consumes more locale and power. To overcome the inconveniences, design another taking care of unit, Vedic multiplier with square root carry select adder (SQRT-CSLA). The proposed design beats the disadvantages of the current structure, and it's similarly giving better introduction of the entire association. The Activation work unit was designed by sigmoid neurons measure. Entire dealing with unit was realized and affirmed by using Verilog HDL language.

III. EXISTING METHOD

VEDIC MATHEMATICS

Vedic-mathematics is a particularly old technique that can be direct used to various pieces of mathematics, for instance, polynomial math, calculating, etc It reduces the multifaceted nature by disposing of the trivial advances while finding out any result. There are 16 sutras in Vedic-mathematics. The going with overview shows the summary of each and every Vedic sutra.

1. (Anurupye) Shunyamanyat
2. Chalana-Kalanabyham
3. Ekadhikena Purvena
4. Ekanyunena Purvena
5. Gunakasamuccayah
6. Gunitasamuccayah
7. Nikhilam-Navatashcaramam Dashatah
8. Paraavartya-Yojayet
9. Puranapuranabyham
10. Sankalana-vyavakalanabhyam
11. Shesanyankena-Charamena
12. Shunyam-Saamyasamuccaye
13. Sopantyadvayamantyam
14. Urdhva-Tiryakbhyam
15. Vyashtisamastih
16. Yavadunam

Among the over 16 sutras, Urdhva Tiryakbhyam (UT) and Nikhilam Navatashcaramam Dashatah (NND) are utilized for registering augmentation of any two numbers. For the most part, NND sutra is liked for bigger piece numbers and UT

sutra is liked for more modest piece numbers. Consequently, UT sutra is utilized in this work.

Urdhva Tiryakbhyam (UT)

Urdhva Tiryakbhyam (UT) signifies "vertically and crosswise" [4]. It is utilized for increase of two numbers with any base. Allow us to consider the system for duplicating two 3-cycle numbers say U [2:0] and V [2:0] for instance and C [3:0] indicates the carry, Y [2:0] means the halfway item yield. At that point the accompanying advances are to be followed:

step1: C0Y0 = U0V0
step2: C1Y1 = {(U0*V1) + (U1*V0)} + C0
step3: C2Y2 = {(U0*V2) + (U1*V1) + (U2*V0)} + C1
step4: C3Y3 = {(U1*V2) + (U2*V1)} + C2
step5: C4Y4 = {(U2*V2)} + C3
Hence, the final product = C4Y4Y3Y2Y1Y0

So 21 × 32 = 276.

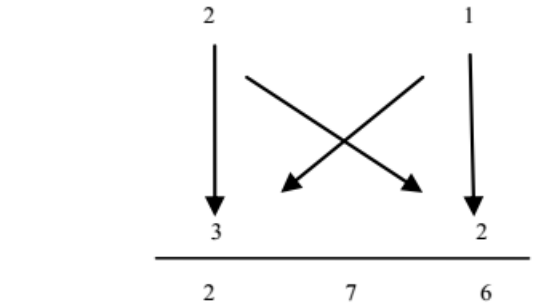


FIG: Multiplication of 21×32 by 'Urdhva Tiryagbhyam' Sutra.

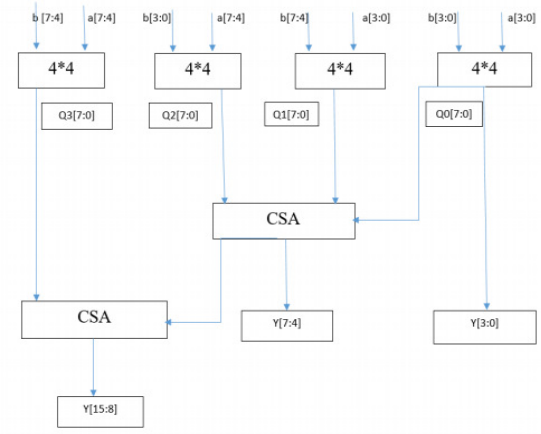


FIG: Urdhva Tiryakbhyam (UT)

BASIC MULTIPLY ACCUMULATOR CIRCUIT (MAC)

In the design of a 16-digit MAC unit, 8 cycle multipliersare utilized. It has been designed by 4bit multipliers. Also, 4bit multiplier is designed utilizing 2-bit multipliers. Fig. shows MAC. The usage of the 2-digit multiplier with half adders utilizing UT sutra is given by Fig.

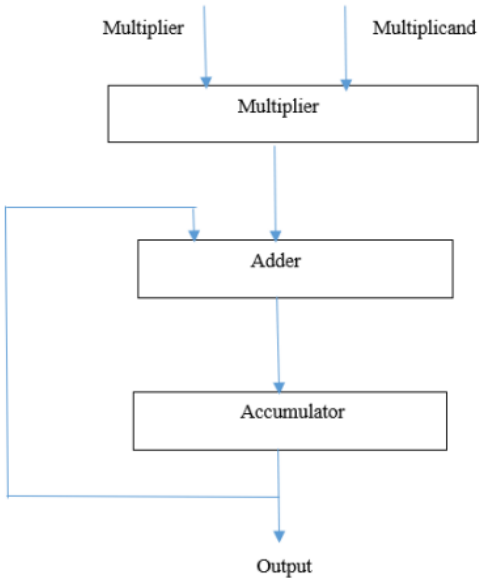


FIG: Basic MAC

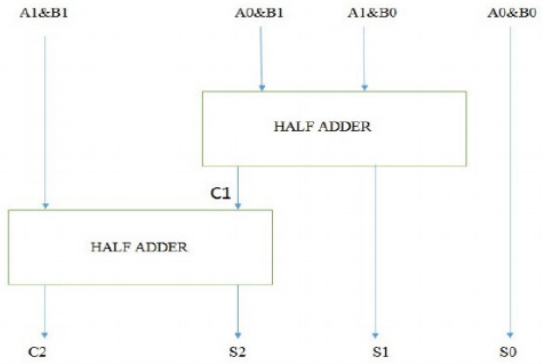


FIG: Implementation of 2-bit multiplier with half adders

CARRY-SAVE ADDER

It is for the most part utilized for processing expansion of at least 3 n cycle numbers. Here, the three sources of info are changed over to two yields where one yield indicates fractional total and the other one addresses carry. The last total is given by moving the carry to left by 1 cycle position and afterward affixing the MSB of incomplete entirety with zeroes.

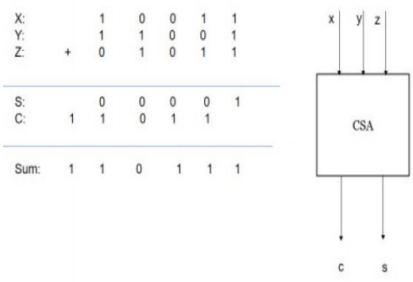


FIG: Carry Save Adder

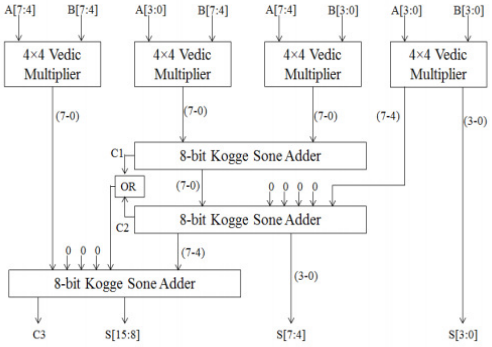
IV. PROPOSED METHOD

Adders:

In hardware, a snake is a digital circuit that performs expansion. Indeed, even the duplication activity relies upon the arrangement of expansion activity.

Adders can be actualized in various manners utilizing various advancements at various degrees of architectures. Design of high velocity and dependable adders is the excellent target and prerequisite for installed applications and separating activity is additionally utilize adders.

PROPOSED BLOCK DIAGRAM:



KOGGE – STONE ADDER (KSA)

KSA is an equal prefix structure carry look forward snake; it is broadly considered as the quickest viper and is generally utilized in the business for superior number-crunching circuits. The total working of KSA can be handily grasped by breaking down it regarding three unmistakable parts.

There are three phases of the calculation in PPA.

- Pre-processing.
- Prefix.
- Final computation.

Pre-Processing:

Pi = Ai XOR Bi

Gi = Ai AND Bi

Prefix:

The dark cell takes two sets of produce and spread signals (Gi, Pi) and (Gj, Pj) as info and figures a couple of create and proliferate signals (G, P) as yield

G = Gi OR (Pi AND Pj)

P = Pi AND Pj

Grey Cell:

The dark cell takes two sets of create and spread signals (Gi, Pi) and (Gj, Pj) as information sources and registers a produce signal G, as yield.

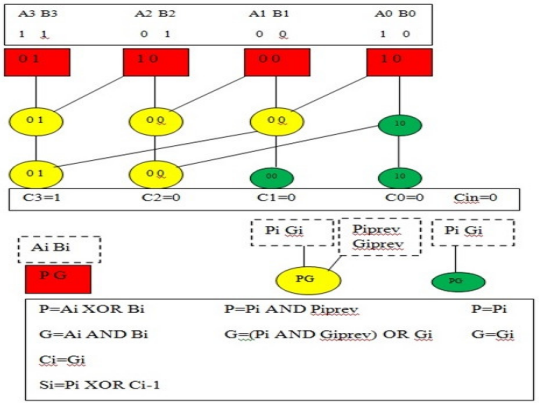
G = Gi OR (Pi AND Pj)

Final computation:

It includes calculation of whole pieces. Total pieces are processed by the rationale given beneath:

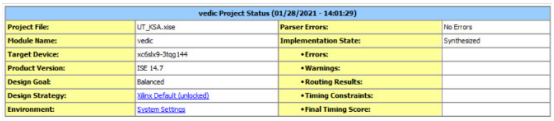
Si = Pi XOR Ci-1

KOGGE STONE ADDER DIAGRAM:



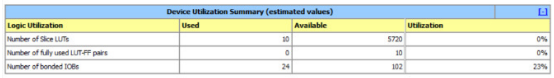
V. RESULTS AND DISCUSSION

The proposed 8bit Vedic-multiplier is implemented inVerilog HDL and simulated in Xilinx Vivado, then synthesisis carried out in Xilinx ISE Design suite. Using this, a 16-bitMAC is also designed.



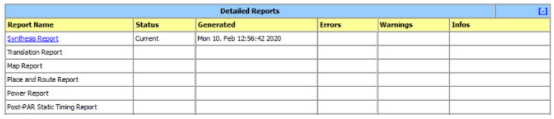
vedic Project Status (01/28/2021 - 14:01:29)

Project File:	UT_KSA.xise	Parser Errors:	No Errors
Module Name:	vedic	Implementation State:	Synthesized
Target Device:	xc6slx9-3tqg144	• Errors:	
Product Version:	ISE 14.7	• Warnings:	
Design Goal:	Balanced	• Routing Results:	
Design Strategy:	Xilinx Default (unlocked)	• Timing Constraints:	
Environment:	System Settings	• Final Timing Score:	



Device Utilization Summary (estimated values)

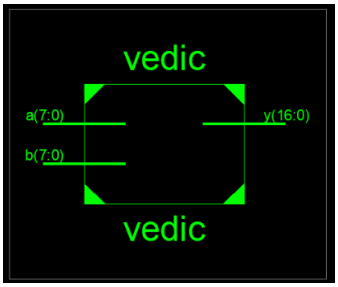
Logic Utilization	Used	Available	Utilization
Number of Slice LUTs	10	5720	0%
Number of fully used LUT-FF pairs	0	10	0%
Number of bonded IOBs	24	102	23%



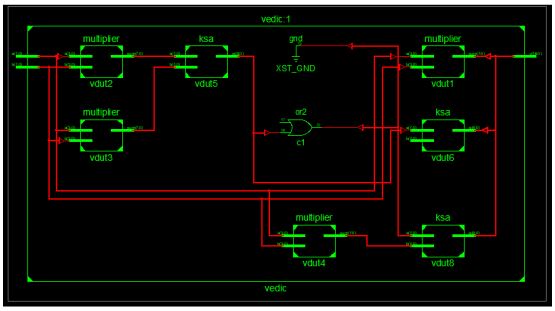
Detailed Reports

Report Name	Status	Generated	Errors	Warnings	Infos
Synthesis Report	Current	Mon 10. Feb 12:56:42 2020			
Translation Report					
Map Report					
Place and Route Report					
Power Report					
Post-PAR Static Timing Report					

Proposed Top Level Module:



Proposed RTL Schematic:



SIMULATION:

Timing Analysis (Proposed System):

```
Delay:               20.338ns (Levels of Logic = 17)
  Source:            a<2> (PAD)
  Destination:       y<16> (PAD)

  Data Path: a<2> to y<16>
                                Gate     Net
    Cell:in->out      fanout    Delay    Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             18    1.222   1.154  a_2_IBUF (a_2_IBUF)
     LUT2:I0->O             2    0.203   0.981  vdut1/p91 (vdut1/p9)
     LUT6:I0->O             3    0.203   0.651  vdut1/g26/hcarry1 (vdut1/c3)
     LUT4:I3->O             3    0.205   0.879  vdut1/g27/g191_xo<0>1 (vdut1/w2)
     LUT6:I3->O             2    0.205   0.961  vdut1/g29/hcarry1 (vdut1/c6)
     LUT6:I1->O             3    0.203   0.879  vdut1/g30/g191_xo<0>1 (vdut1/w4)
     LUT6:I3->O             3    0.205   0.651  vdut1/g32/hcarry1 (vdut1/c9)
     LUT3:I2->O             2    0.205   0.617  vdut1/g33/g191_xo<0>1 (vdut1/w6)
     LUT5:I4->O             2    0.205   0.864  vdut1/g34/out1 (vdut1/c11)
     LUT6:I2->O             2    0.203   0.961  vdut1/g35/g191_xo<0>1 (y1<6>)
     LUT6:I1->O             3    0.203   0.995  vdut6/ci<2>1 (vdut6/ci<2>)
     LUT6:I1->O             3    0.203   1.015  vdut6/ci<4>1 (vdut6/ci<4>)
     LUT6:I0->O             3    0.203   0.651  vdut6/ci<6>1 (vdut6/ci<6>)
     LUT4:I3->O             2    0.205   0.961  c1 (c)
     LUT5:I0->O             4    0.203   0.684  vdut8/ci<4>1 (vdut8/ci<4>)
     LUT3:I2->O             1    0.205   0.579  vdut8/Mxor_si<6>_xo<0>1 (y_14_OBUF)
     OBUF:I->O                   2.571          y_14_OBUF (y<14>)
    ----------------------------------------
    Total                       20.338ns (6.852ns logic, 13.486ns route)
                                         (33.7% logic, 66.3% route)
```

VI. CONCLUSION

A 16-digit MAC unit using a 8-cycle Vedic-multiplier with carry save snake was designed. It depended on UT sutra and coded in Verilog HDL. The usage was carried on Artix-7 FPGA. It was seen to have around 9.5% force decrease alongside critical improvement in zone and delay. An examination with an ordinary multiplier and existing multiplier was completed separately. The MAC unit designed with the proposed multiplier can be utilized in DSP applications for improving the speed and execution. In future, this work can be stretched out by supplanting the multipliers with reversible rationale doors for accomplishing further force decrease and better execution.

- By Comparing both the Existing vedic multiplier and proposed vedic multiplier, it is seen that Proposed vedic multiplier streamlines the delay.
- So, it is inferred that, multiplier which requires quick usage can utilize this kind of multiplier in picture and signal preparing applications.

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