# Performance Improvement of Carry Look Ahead Adder

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**Abstract- Adder is the major component in all data path unit. In this paper, designing of fast adder has been done by carry look ahead adder(CLA) instead of ripple carry adder(RCA) since RCA has the worst propagation delay of carry bit. By reducing the number of MOS and FET, the power usage of circuit would positively be reduced. In this paper, we design a 4-bit CLA adder with smaller size and dropping down the power consumption, by improving the basic logic of the circuit that is, by trying pseudo NMOS logic, pass transistor and transmission gate logic. This architectural replacement will improve the size and propagation delay. By using Cadence Virtuoso tool each parameter can be calculated.**

**Keywords – CLA (carry lookahead adder), RCA (ripple carry adder), Pseudo NMOS logic, Pass transistor logic, Transmission gate logic.**

## I. INTRODUCTION

Arithmetic operations such as addition, subtraction, multiplication and division are widely used and play an important role in various digital systems such as digital signal processor (DSP) architecture, microprocessor and microcontroller and data process unit. Adders are the logic circuits designed to perform high speed arithmetic operations and are important components in digital systems because of their extensive use in other basic operations such as subtraction, multiplication and division. In many computers and other kinds of processors, adders are used not only in the arithmetic logic unit, but also in other parts of the processor, where they are used to calculate addresses, table indices, and same kind of operations. This VLSI system requires fast addition which impacts the overall performance of digital system. These addition operations are done by using adders. Various adder structures can be used to execute addition, such as serial and parallel structures and most of researches are done on the design of high-speed, low-area, or low-power adders. CLA are very important building block for any digital circuits. In this paper, the CLA has been implemented using different logic style like standard CMOS, Pseudo NMOS logic Pass

Transistor Logic (PTL) and Transmission gate logic. Transistor simulation results has been done for the feature size of 180nm to determine the propagation delay, average power consumption and their Power delay product (PDP). The rest of the paper is organized as follows. Comparison of CLA and RCA are explained in section II. Comparison parameters are presented in section III. Basics of CLA are presented in section IV. Implementation of CLA using various logics is explained in section V. Proposed system is presented in section VI. Simulation Results are given in section VII. Concluding remarks are given in section VIII.

## II. COMPARISON OF CLA AND RCA

Full Adder cell is the basic cell for addition of two binary bits. However, in modern processors, implementation of wide adders is required. Ripple Carry Adder (RCA) based on 1-full adder is the basic technique for implementation of wide adders. However, propagation delay obtained using RCA in long carry chains is quite high for which it became quite impractical to use RCA in high performance devices. In order to solve the carry propagation delay in long carry chains, several Parallel-Prefix Adder topologies have been developed. CLA adder is one of the Parallel Prefix Adder (PPA) topologies which reduces carry propagation delay by using a complex circuitry involving carry-propagate and carry-generate terms. Although, CLA adder enhances performance in speed by reducing propagation delay, transistor count is quite high in CLA adder compared to RCA. This high transistor count results in high area consumption in chip. In addition, it results in high power dissipation, Static CMOS logic based CLA adders are most common and widely used adder topology due to its high robustness and driving power. However, using complementary pair of N-channel CMOS (NMOS) and P-channel CMOS (PMOS) makes the number of transistors in circuit high. This high number of transistors accounts for high input impedance for signals.

## III. COMPARISON PARAMETERS

### *3.1 Propogation Delay –*

Propagation delay of a logic gate is defined as the time it takes for the effect of change in input to be visible at the output. In other words, propagation delay is the time required for the input to be propagated to the output. It can be computed as the ratio between the link length and the propagation speed over the specific medium. Propagation delay is equal to d / s where d is the distance and s is the wave propagation speed. In wireless communication, s = c, i.e, the speed of light.

### *3.2 Area –*

Area is calculated by the number of transistor present in the circuit.

### *3.3 Power Dissipation –*

The total power dissipation in a CMOS circuit can be expressed as the sum of two main components:

- Static power dissipation (due to leakage current when the circuit is idle):
  When a CMOS circuit is in an idle state there is still some static power dissipation–a result of leakage current through nominally off transistors. Both nMOS and pMOS transistors used in CMOS logic gates have finite reverse leakage and sub-threshold currents. In a silicon chip there are millions of transistors and the overall power dissipation due to leakage current is comparable to dynamic power dissipation. The values of leakage and sub-threshold currents depend upon processing parameters.

- Dynamic power dissipation (when the circuit is switching):
  Dynamic power dissipation occurs when the MOS transistor switches to charge and discharge the output load capacitance at a particular node at operating frequency.

## IV. BASICS OF CLA

The principle of 4-bit CLA is to calculate the carry-in of each bit from inputs directly. For addition with two inputs, the external carry-in is denoted as C0. Both inputs have 4 bits and they are represented as A3A2A1A0 and B3B2B1B0 respectively. Then sum of this addition S3S2S1S0 can be calculated by Full adders. Thus S3S2S1S0 = A3A2A1A0 ⊕ B3B2B1B0 ⊕ C3C2C1C0, where C3 C2 and C1 are the carry-outs of previous bits. The logic relationships between the carry-outs and inputs are expressed by equations (1)-(3). Among them, signals Carry-Propagation (abbreviated Pi) and Carry-Generate (abbreviated Gi) are obtained Pi = Ai ⊕ Bi and Gi = Ai & Bi AiBi, in which i is the value 0 1 2 or 3. The symbol '&' representes logic AND and it can be omitted in function sometimes. Besides, the symbol '+' denotes the logic OR.

$$C_1 = G_0 + P_0C_0 \quad (1)$$

$$C_2 = G_1 + P_1G_0 + P_1P_0C_0 \quad (2)$$

$$C_3 = G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_0 \quad (3)$$

$$G = G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0 \quad (4)$$

$$P = P_3P_2P_1P_0 \quad (5)$$

In equations (4) and (5), G represents the carry-propagation signal of the 4-bit CLA adder and P is denoted as the carry-generate signal. Based on them, carry-out of this addition $C_4$ is given by formula; $C_4 = G + PC_0$. The logic gate level implementation of 4-bit CLA using basic AND and XOR gates s shown in fig 4.1.

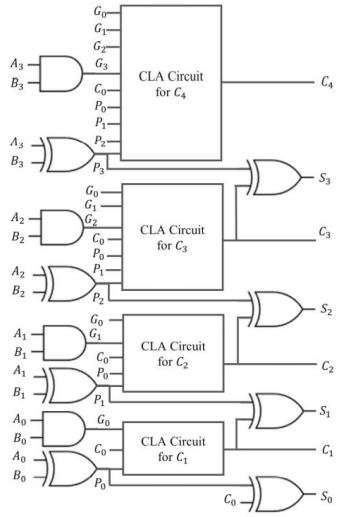
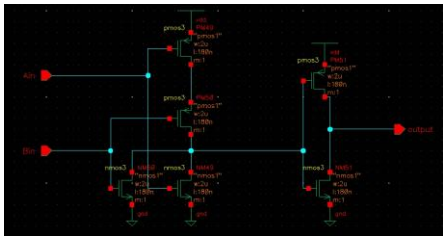



Figure 1. Implementation of CLA using basic logic gates.

## V. IMPLEMENTATION OF CLA USING VARIOUS LOGICS

*5.1 Implementation using Static CMOS* –

Static CMOS is a logic circuit design technique whereby the output is always strongly driven due to it always being connected to either VCC or GND (except when switching).



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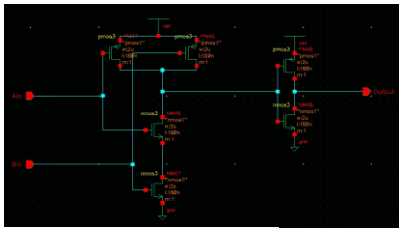

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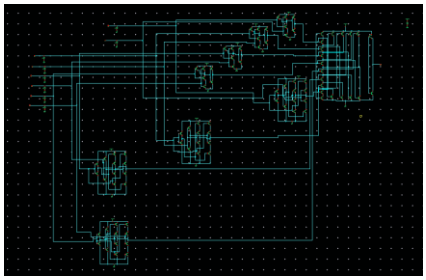

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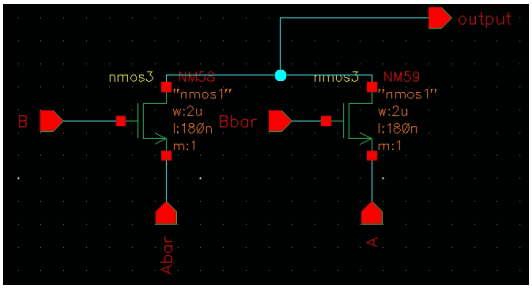
Figure 2. (a) AND gate implementation (b) XOR gate implementation (c) CLA implementation

*5.2 Implementation using pseudo NMOS –*

Pseudo NMOS is an inverter that uses a p-device pull-up or load that has its gate permanently ground and an n-device pull-down or driver is driven with the input signal. This roughly equivalent to use of a depletion load is NMOS technology and is thus called 'Pseudo-NMOS'. The circuit is used in a variety of CMOS logic circuits. In this, PMOS for most of the time will be linear region. So resistance is low and hence RC time constant is low. When the driver is turned on a constant DC current flows in the circuit. The CMOS pull up network is replaced by a single pMOS transistor with its gate grounded. Since the pMOS is not driven by signals, it is always 'on'. The effective gate voltage seen by the pMOS transistor is Vdd. Thus the overvoltage on the p channel gate is always Vdd -VTp. When the nMOS is turned 'on', a direct path between supply and ground exists and static power will be drawn. However, the dynamic power is reduced due to lower capacitive loading.

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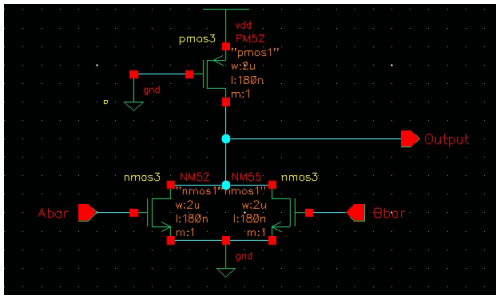


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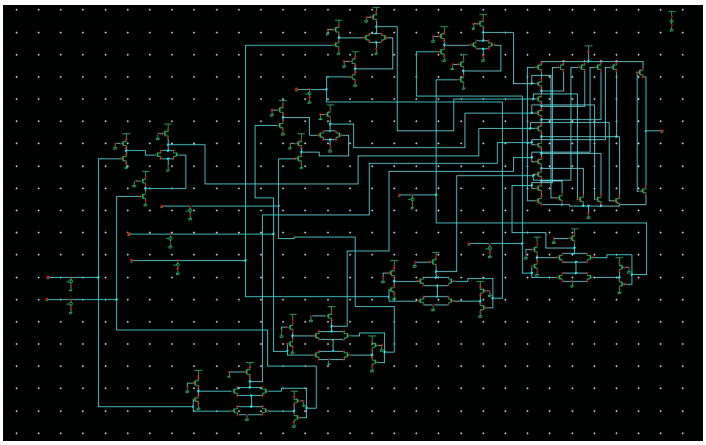

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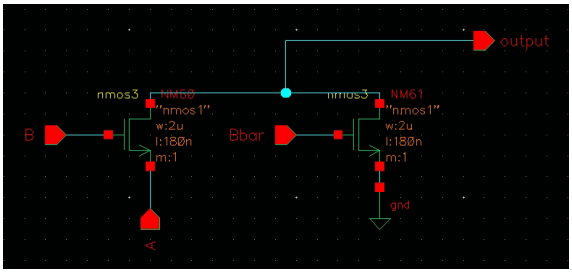
Figure 3. (a) AND gate implementation (b) XOR gate implementation (c) CLA implementation

*5.3 Implementation using Pass Transistor Logic –*

Pass transistor logic (PTL) describes several logic families used in the design of integrated circuits. It reduces the count of transistors used to make different logic gates, by eliminating redundant transistors. Transistors are used as switches to pass logic levels between nodes of a circuit, instead of as switches connected directly to supply voltages. This reduces the number of active devices, but has the disadvantage that the difference of the voltage between high and low logic levels decreases at each stage. Each transistor in series is less saturated at its output than at its input. If several devices are chained in series in a logic path, a conventionally constructed gate may be required to restore the signal voltage to the full value. By contrast, conventional CMOS logic switches transistors so the output connects to one of the power supply rails, so logic voltage levels in a sequential chain do not decrease. Simulation of circuits may be required to ensure adequate performance.

The pass transistor is driven by a periodic clock signal and acts as an access switch to either charge up or charge down the parasitic capacitance C*x*, depending on the input signal V*in*. Thus there is two possible operations, when the clock signal is active (CK = 1) are the logic "1" transfer (charging up the capacitance C*x* to a logic-high level) and the logic "0" transfer (charging down the capacitance C*x* to a logic-low level). In either case, the output of the depletion load nMOS inverter obviously assumes a logic-low or a logic-high level, depending upon the voltage V*x*.

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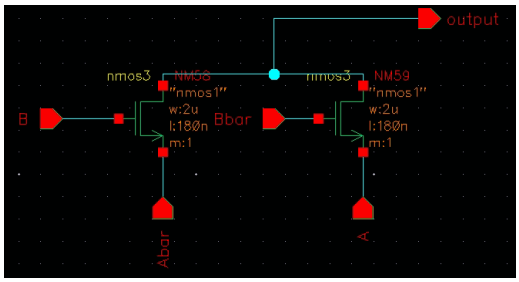


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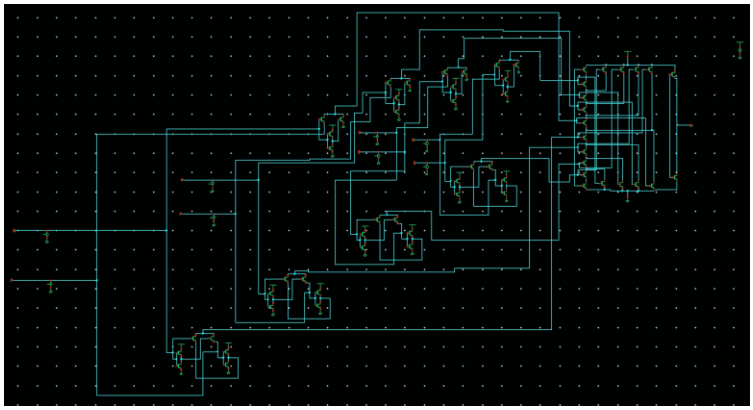

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Figure 4. (a) AND gate implementation (b) XOR gate implementation (c) CLA implementation

## VI. PROPOSED LOGIC

*6.1 Implementation using Transmission gate logic -*

The proposed circuit is implemented using transmission gate logic. A transmission gate (TG) is an analog gate similar to a relay that can conduct in both directions or block by a control signal with almost any voltage potential. It is a CMOS-based switch, in which PMOS passes a strong 1 but poor 0, and NMOS passes strong 0 but poor 1. Both PMOS and NMOS work simultaneously.

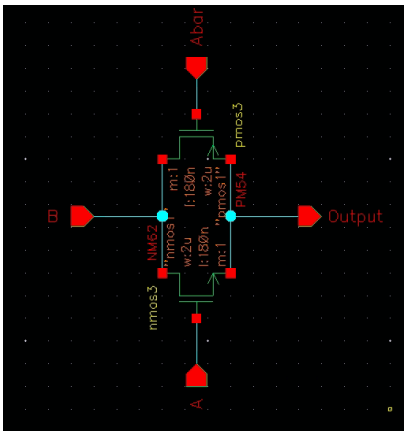
When the control input is a logic zero (negative power supply potential), the gate of the n-channel MOSFET is also at a negative supply voltage potential. The gate terminal of the p-channel MOSFET is caused by the inverter, to the positive supply voltage potential. Regardless of on which switching terminal of the transmission gate (A or B) a voltage is applied (within the permissible range), the gate-source voltage of the n-channel MOSFETs is always negative, and the p-channel MOSFETs is always positive. Accordingly, neither of the two transistors will conduct and the transmission gate turns off.

When the control input is a logic one, the gate terminal of the n-channel MOSFETs is located at a positive supply voltage potential. By the inverter, the gate terminal of the p-channel MOSFETs is now at a negative supply voltage potential. As the substrate terminal of the transistors is not connected to the source terminal, the drain and source terminals are almost equal and the transistors start conducting at a voltage difference between the gate terminal and one of these conducts.

One of the switching terminals of the transmission gate is raised to a voltage near the negative supply voltage, a positive gate-source voltage (gate-to-drain voltage) will occur at the N-channel MOSFET, and the transistor begins to conduct, and the transmission gate conducts. The voltage at one of the switching terminals of the transmission

gate is now raised continuously up to the positive supply voltage potential, so the gate-source voltage is reduced (gate-drain voltage) on the n-channel MOSFET, and this begins to turn off. At the same time, the p-channel MOSFET has a negative gate-source voltage (gate-to-drain voltage) builds up, whereby this transistor starts to conduct and the transmission gate switches.

Thereby it is achieved that the transmission gate passes over the entire voltage range. The transition resistance of the transmission gate varies depending upon the voltage to be switched, and corresponds to a superposition of the resistance curves of the two transistors.

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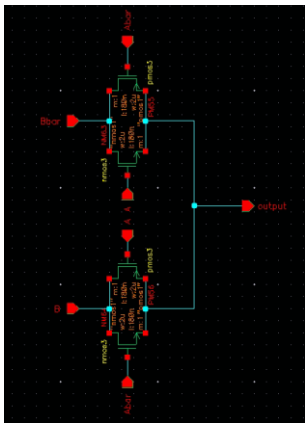


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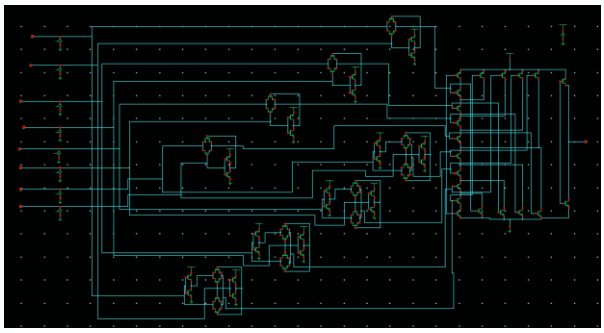

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Figure 5. (a) AND gate implementation (b) XOR gate implementation (c) CLA Implementation

## VII. SIMULATION RESULTS

The comparison of 4-bit CLA implemented in four logic designs are done in channel length 180nm technology. Power dissipation, transistor count, and propagation delay are calculated and compared.

Table 1- Simulation Result

| Logic | Transistor Count | Delay(s) | Average Power(µW) |
|---|---|---|---|
| Static CMOS | 248 | $25.6x10^{-9}$ | 3.502 |
| Pseudo NMOS | 176 | $30.08x10^{-9}$ | 13.86 |
| Pass Transistor | 132 | $21.81x10^{-9}$ | 8.62 |
| Transmission Gate | 136 | $17.5x10^{-9}$ | 2.296 |

## VIII. CONCLUSION

The proposed CLA is designed using transmission gate technology and it performed with 31.6% less propagation delay and 34.4% less power dissipation. The transistor count is also reduced to an average of 112 transistors as compared to the conventional CMOS circuit.

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