Design of Buck Converter with Power Stage Resistances

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Abstract

Voltage regulators are mainly used to regulate the voltage to different levels based on the need of the application. Switching Voltage regulators are most used in the industry today due to their various advantage especially the DC-DC converters are the best SMPS regulators in the market and most widely used in the SOC. These Converters are of three types Buck, Boost, Buck- Boost. This paper mainly focuses on the Buck Converter design requirements with non-idealities. Here, the duty cycle with power stage resistances is 0.098 whereas steady state duty cycle is 0.095 which shows that the input voltage reduces, and duty cycle increases in non-ideal condition. The efficiency of the VR is seen as 94.86% which depends on the power loss components. The voltage undershoot of 148.10mV is a result of sudden change of Inductor current ramp up. Inductor and capacitor selection is made based current ripple and output voltage ripple. Spice simulation is used to verify this design and all the above parameters are seen in form of waveform.

Keywords

DC-DC Converters, Buck Converters, Voltage Undershoot, Duty Cycle, Power Loss, Efficiency.

Introduction

Modern electronic applications require the ability to handle large electrical fluctuations. Electronic equipment's are being widely used among the industries and induvial and most of these electronic devices need a step-down converter or a voltage regulator. A voltage regulator is a circuit that produces and maintains a constant output voltage regardless of input voltage or load conditions. The voltages from a power source are kept within a range that is compatible with the other electrical components by voltage regulators (VRs). Voltage regulators are used for DC/DC conversion, AC/AC or AC/DC power conversion. VR is mainly categorized into two: Linear Regulators and Switching Regulators. Usually the latter is most often used due to higher efficiency and wide applications of switching. One of the most popular Switching Regulator are DC- DC Converters. These are further categorized into three types of converters Buck Converter which convert high Input voltage to a lower volage. Boost Converters to convert lower input voltage to higher output voltage and Buck Boost converters that act as both for conversion to either higher output voltage or lower output voltage based on the application, these Buck Boost converters are mostly used in Battery related applications.

Buck Converters are step-down converters. It has components such as MOSFETs, Inductor, Capacitor, and voltage source. Due it's wide array of applications in various industries there is active research in this area. Existing research done especially in the design and simulation of dc-dc converters shows the theoretical derivations and parameters equations with design and examples. Simulation results for buck, boost and buck-boost converters are shown with the chance of different input parameters.[1] These input parameters not only effect the component selection but also converter performance, as discussed in [2] about ESR impacting the COT performance. Transient response is a major drawback in a buck converter which causes voltage overshoot and undershoot. There are many converters as discussed in [3-11] which provides information on the impact and working of the converter for fast transient response. From the existing work done in converters such as Voltage mode control, current mode control, Non-Linear ADC, Time Optimal Control, Power

Management IC and Constant on Time Converter (COT). COT has been the most widely used converter in the industry due it's performance and efficiency [12].

The previous work suggests the design methods and equations for a Buck Converter in steady state but this paper shows in detail the design of a Buck Converter with non-ideal components by considering FET resistances, capacitor ESR, and Inductor ESL as these non-idealities affect various parameters of Buck converter designing which changes the efficiency, voltage and current ripple. This paper also shows the change in parameter values in both steady state and actual state thereby showing the effect of non-ideal components on the performance and efficiency of the converter.

1. Working of Buck Converter

There are ideally two cases in a buck converter once when the switch is open and the other when switch is closed which is seen in the below cases with reference to Figure 1.

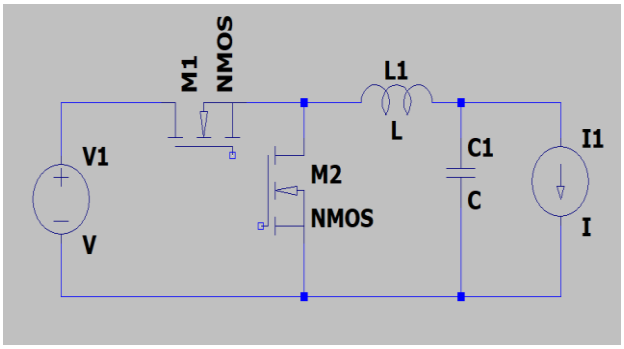

Figure 1: Buck Converter Circuit Design

Case 1: When the switch(M1) is turned on, the current flows to the output capacitor, charging it up. And the inductor is also energized in this cycle. Since the voltage across the capacitor cannot rise instantly, and since the inductor limits the charging current, the voltage across the cap during the switching cycle is not the full voltage of the power source.

Case 2: When the switch (M2) is turned off, since the current in an inductor cannot change suddenly, the inductor creates a voltage across it. This voltage charges the capacitor and powers the load through MOSFET(M2) when the switch is turned off, maintaining output current throughout the switching cycle.

2. Design of Buck Converter

Unlike a steady state Buck Converter using ideal components, a non-ideal Buck Converter is mostly a Converter with non-ideal components that is both the top side FET(M1) and Bottom side FET(M2) have resistances R1 and R2 respectively in series. There exists an Inductor DC-Resistance (DCR) R3 and Capacitor ESR. Apart from these there can be many other non-idealities based on circuit design and the application. This section shows the designing of inductor based on the above discussed non- idealities.

2.1 Duty Cycle:

The key to determining the Duty ratio is to look at the inductor current and voltage first for the closed D switch and then for the open switch (1-D). In Ideal conditions of the Buck Converter, the duty cycle of the Buck Converter can be calculated as follows:

$$D = \frac{VOUT}{VIN} \quad (1)$$

ON Time and OFF Time can also be calculated using duty cycle and Total Time delay.

$$Ton = D \times T \quad (2)$$

$$Toff = T - Ton \quad (3)$$

As seen above for steady state, the total change in the inductor current over one time period is zero. But, if a buck converter with non-idealities is considered i.e resistances like series resistances R1(Top side FET resistance), R2(Bottom side FET Resistance) and resistance R3 in series with the inductor is also considered.

Therefore, we consider that inductor current in both the on and off case will be equal.

$$\Delta I_{L\text{-}ON} + \Delta I_{L\text{-}OFF} = 0 \quad (4)$$

Applying KVL, to the above given circuit, we can obtain the following equation:

$$(VIN - V0 - I_L \times R1 - I_L \times R3)\, TON = (V0 + I_L\,(R2 + R3))\, TOF \quad (5)$$

Replacing TON and TOFF equations:

$$(VIN - V0 - I_L \times R1 - I_L \times R3)\, D \times T = (V0 + I_L\,(R2 + R3)) \times (1\text{-}D) \times T \quad (6)$$

On further solving the above equation, the duty cycle for a buck converter with Power Stages can be obtained:

$$D = \frac{V0 + I\,(R2 + R3)}{VIN - I\,(R1 + R2)} \quad (7)$$

2.2 Inductor Selection

The current through the inductor (I_L) has the average current which is equal to load current and ripple current(which is caused due to input and output switching). [6]

$$V = L\frac{di}{dt} \quad (9)$$

$$I = \frac{1}{L}\int V dt \quad (10)$$

$$I_{ripple} = \frac{1}{L} V\, \Delta t \quad (11)$$

When the inductor is in charging mode the voltage across the inductor is Vin -Vout and Δt is the time switch S1 is closed and when the inductor is discharging, V is simply Vout and Δt is the time S2 is closed.

Ideally, if assumed there is no voltage drop across the switches, I_{ripple} remains the same for both the cases that is when the switch S1 is open and when the switch S2 is closed.

$$I_{ripple} = \frac{1}{L}(V_{in} - V_{out})\, \Delta t_{s1} = \frac{1}{L} V_{out}\, \Delta t_{s2} \quad (12)$$

$$\frac{Vout}{Vin} = \frac{\Delta ts1}{\Delta ts1 + \Delta ts2} \quad (13)$$

From we can choose values for the inductor and the switching frequency. The switching frequency is the maximum number of switching operations per second. In other words, switching frequency is a measure of how often the MOSFET switches on and off per second. The switching frequency is given in Hz. It is an important factor to measure the power loss of a buck converter.

It is given by $f_{sw} = \frac{1}{T}$ (14)

Notice that for a given current and voltage difference, the inductor value is proportional to Δt.Which means that greater the switching frequency, lower is the required inductor value.
Therefore, the inductor value can be selected based on Equation 15.

$$L = \frac{(Vin - Vout)\,\Delta t}{Iripple} \quad (15)$$

2.3 Capacitor Selection

The main criteria for selecting a capacitor is it's ESR and capacitance. Since the ESR of the capacitor affects the efficiency and performance. The best choice would be a capacitor with low ESR. The capacitors are chosen to meet the output voltage ripple specification. In steady state conditions, assuming negligible voltage ripple the following Equation 16 is valid

$$\Delta V = \frac{Vin \times D(1-D)}{8LCf^2} \quad (16)$$

Since, the design is for non-ideal conditions, output ripple voltage is usually a composite waveform created by ripple current of Inductor passing through capacitance. Therefore, if the ESR of capacitance and ESL of Inductor is taken into consideration.

$$\Delta V = \Delta I_L \left(\frac{1}{8 \times C \times fsw} + ESR\right) + ESL\left(\frac{V_{in}}{L}\right) \quad (17)$$

2.4 Voltage Undershoot

Transient response is essentially a response to the load transients that happens when load current rapidly changes from one value to another. The VR may not be able to instantly react to such instant changes. Therefore, the load current is supplied with energy from the inductor as well as the output capacitor. Since, the capacitor drains all it's energy momentarily to supply the load current, there is a output voltage drop and it continues until the inductor current reaches the normal value. This voltage drop is also known as voltage undershoot. As a solution to this problem, we use various different controllers.

The calculation of the voltage undershoot can be done, considering the rapid change of inductor current from time t1 to t2 or from 0 to some value. Which results in the voltage drop of the capacitor.

$$C\Delta V = \int_{t1}^{t2} i\, dt \quad (18)$$

$$\Delta V = \frac{i(t_2 - t_1)}{C} \quad (19)$$

2.5 Efficiency

In steady state the efficiency can be calculated as the ratio of Output Power to the ratio of Input Power which is given by the equation:

$$\eta = \frac{VOUT \times IOUT}{VIN \times IIN} \quad (20)$$

In an actual converter there may be many losses such as , Conduction loss, Switching Loss, Conduction Loss due to Inductor , Switch node loss of capacitance, Dead Time loss, Inductor loss, Magnetic Loss, Gate Charge Loss. These power losses of various components affect the performance and efficiency of the Converter. Which can be given by below Equation 12.

$$\eta = \frac{VOUT \times IOUT}{VOUT \times IOUT + P} \quad (21)$$

3. RESULTS

The design considerations can be taken as input voltage of 12V and two MOSFETs with Rds(on) values as 0.4 mΩ. The Inductor value can have an inductance of 300nH and the DCR could be given manually. The capacitance value of 810uF can be selected. A range of capacitors are available and based on the application, user can choose either ceramic, bulk or any other type of capacitor with required ESR based on the output ripple. Once these components are selected, a load of 10A can be given with a small resistance in parallel for design purpose.Many simulation tools can be used to

verify the design. Here, the LTspice simulation software toll has been used. Once a buck converter is designed with above specifications the transient analysis is done with a stop time of 1millisec. The following waveforms can be observed once the design is simulated.

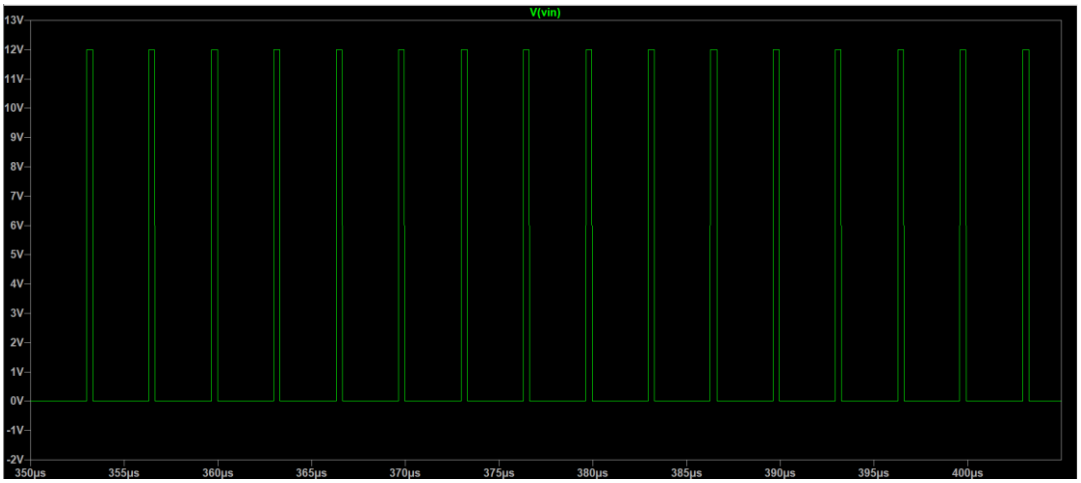

Figure 2: Input Voltage showing TON and TOFF

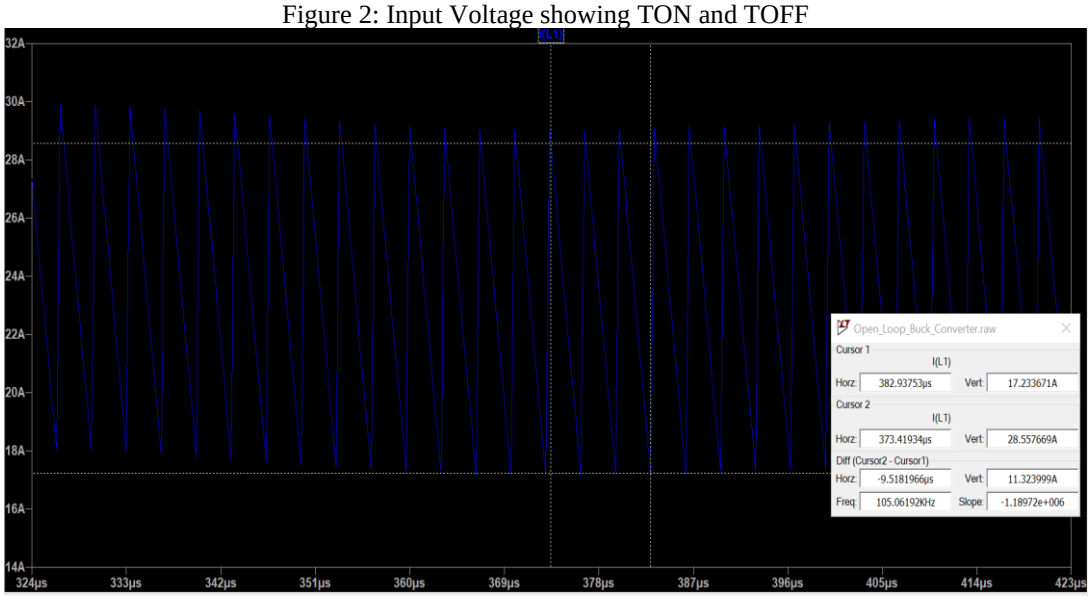

Figure 3: Inductor p-p ripple current

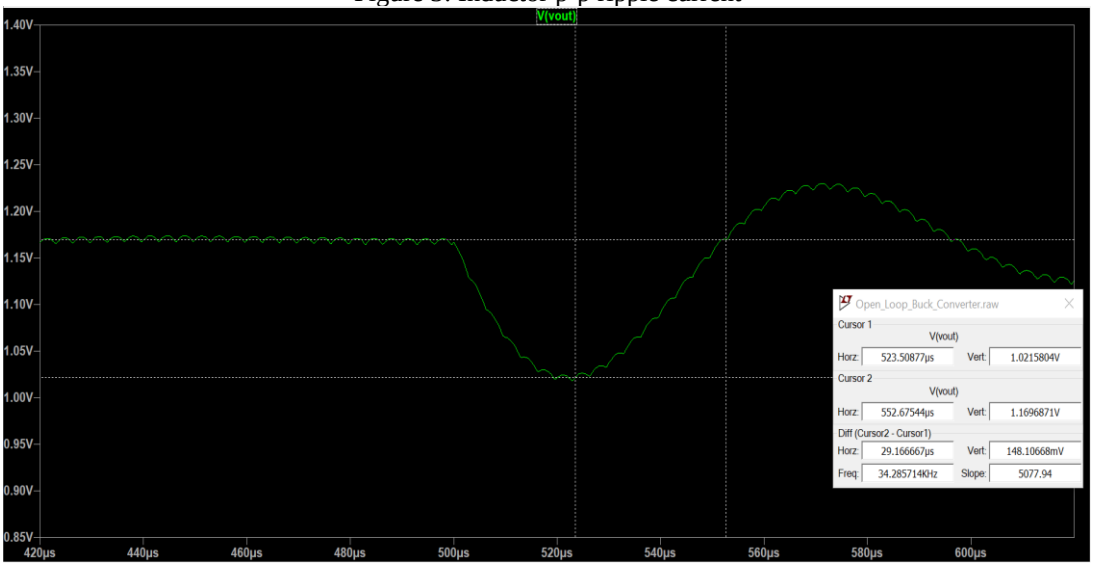

Figure 4: Voltage Undershoot

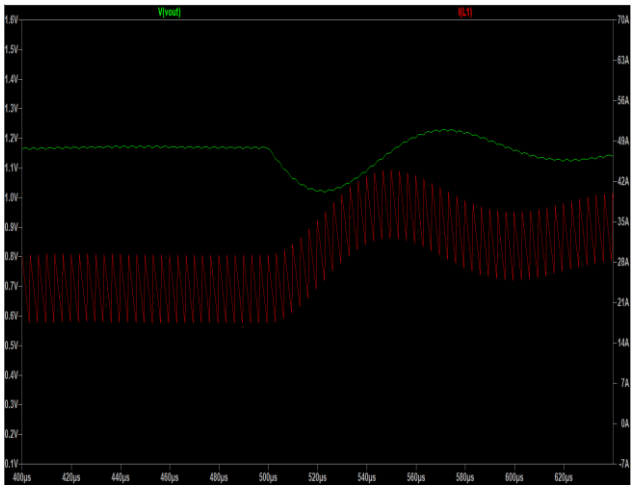

Figure 5: Voltage Undershoot with Current Ramp up

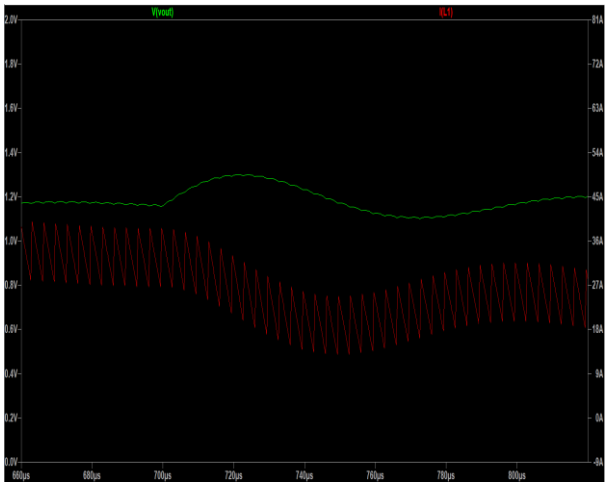

Figure 6 :Voltage Overshoot with Current Ramp down

Table1: VR Design Result Parameters

	PARAMETER	VALUE
1.	Input Voltage	12V
2.	Output Voltage	1.15V
3.	Switching Frequency	300KHz
4.	Time Period	3.33 usec
5.	Duty Cycle	0.095
6.	Duty cycle with resistances	0.098
7.	ON Time	0.33 usec
8.	OFF Time	1.33 usec
9.	Inductor	300nH
10.	Capacitor	810uF
11.	I(p-p) ripple	11.32A
12.	Voltage Undershoot	148.10mV
13.	Voltage Overshoot	146.06mV
14.	Total Power Loss	6.5W
15.	Efficiency	94.86%

Figure 2 shows the ON Time and OFF Time of the converter which is the same as the calculated value. Inductor p-p ripple current can be observed from Figure 3 which is mainly based on the inductor 300nH chosen here. Figure 5 shows the inductor current ramp up from t1 to t2 that is 49.85usec and a voltage undershoot of 148.10Mv is observed. Similarly in Figure 6 the inductor current rapidly ramps down from t1 to t2 and a voltage overshoot 0f 146.06mV is observed.

4. CONCLUSION

The On time and Off time are majorly impacted by the duty cycle. The inductor current ripple is directly dependent on duty cycle and output voltage and inversely dependent on Inductor value. Therefore, smaller the inductor lesser the Inductor ripple. Similarly, the voltage ripple is also affected by the Capacitance and it's ESR. Therefore, capacitance with the least ESR is chosen. Voltage Undershoot is directly proportional to the sudden change in Inductor Current. As a solution to this, a fast-transient response can be provided using converters like Voltage Control Mode, Current Mode Control, Time Optimal Control, Non-Linear ADC and Adaptive Constant On Time Controller. Power loss components majorly effects the Converter Efficiency to minimize these losses and improve the efficiency , few losses like inductor loss can be minimized by reducing the hysteresis loss or it can be reduced by choosing an appropriate capacitor as it's ESR and capacitance value can also impact. The power MOSFET plays an important role in the power dissipated. A more efficient VR Design can be made considering the above points.

REFERNCES

1. Lopa SA, Hossain S, Hasan MK, Chakraborty TK. “Design and simulation of DC-DC converters”. International Research Journal of Engineering and Technology (IRJET). 2016 Jan;3(01):63-70.
2. 2. J. Wang, B. Bao, J. Xu, G. Zhou and W. Hu, "Dynamical Effects of Equivalent Series Resistance of Output Capacitor in Constant On-Time Controlled Buck Converter," in IEEE Transactions on Industrial Electronics, vol. 60, no. 5, pp. 1759-1768, May 2013, doi: 10.1109/TIE.2012.2190956. E. Meyer, Z. Zhang, Y. Liu “An Optimal Control Method for Buck Converters Using a Practical Capacitor Charge Balance Technique,” IEEE Transactions on Power Electronics, Vol. 23, No. 4, July 2008, pp. 1802-1812.
3. Z. Zhao, A. Prodic “Continuous-Time Digital Controller for High- Frequency DC-DC Converters,” IEEE Transactions on Power Electronics, Vol. 23, No. 2, March 2008, pp. 564-573
4. A. Corradini, R. Mattavelli, S. Saggini, “Time Optimal Parameters- insensitive Digital Controller for DC-DC Buck Converters,” IEEE PESC , June 2008
5. N. Andrews, “The Global Market for Power Supply and Power Management Integrated Circuits,” IEEE Applied Power Electronics Conference and Exposition, pp.126-131, Mar. 2002.
6. R. B. Ridley, “A new continuous-time model for current-mode control,” IEEE Trans. Power Electron., vol. 6, pp. 271–280, Apr. 1991.
7. Wei Tang, Fred C. Lee, and Raymond B. Ridley, Small Signal Modeling of Average Current Mode Control‖, IEEE Trans. On Power Electronics, Vol. 8, No.2, April 1993, pp.112-119.
8. A. Prodic, D. Maksimovic, and R. Erickson, “Design and implementation of a digital PWM controller for a high-frequency switching DC–DC power converter,” Proc. IEEE IECON Conf., 2001, pp. 893–898.
9. T. W. Martin and S. S. Ang, “Digital control of switching converters,” Proc. IEEE Int. Symp. Ind Electron., vol. 2, 1995, pp. 480–484
10. Sudharshan KM. Design of peak current mode-controlled Buck converter with high side current sensing technique for overcurrent protection. Turkish Journal of Computer and Mathematics Education (TURCOMAT). 2021 May 23;12(12):2417-25.
11. Bizzarri F, Nora P, Brambilla A. A novel sufficient condition to avoid subharmonic oscillations for buck converters with constant on-time control. Electronics Letters. 2020 Jan 16;56(6):305-8.
12. Lopa SA, Hossain S, Hasan MK, Chakraborty TK. Design and simulation of DC-DC converters. International Research Journal of Engineering and Technology (IRJET). 2016 Jan;3(01):63-70.
13. Hashim A, Bakkaloglu B. Fast transient digitally controlled buck regulator with inductor current slew-rate boost. In2013 IEEE International Symposium on Circuits and Systems (ISCAS) 2013 May 19 (pp. 2944-2947). IEEE.
14. “Control Methods (Voltage Mode, Current Mode, Hysteresis Control)”,TechWeb,2015.12.06 https://techweb.rohm.com/knowledge/dcdc/s-dcdc/02-s-dcdc/97
15. Semiconductor RO. Switching Regulator IC Series «Efficiency of Buck Converter»,
16. Hu W, Yang R, Wang X, Zhang F. Stability Analysis of Voltage Controlled Buck Converter Feed From a Periodic Input. IEEE Transactions on Industrial Electronics. 2020 Mar 25;68(4):3079-89.
17. Sudiharto I, Rahadyan MI, Qudsi OA. Design and Implementation of Buck Converter for Fast Charging with Fuzzy Logic. JAREE (Journal on Advanced Research in Electrical Engineering). 2021 Apr 1;5(1).