VLSI Circuits design using Resonant Rotary Clocking

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Abstract- Resonant clocking technologies are next-generation clocking technologies that offer low or controllable-skew, low-jitter and multi-gigahertz frequency clock signals with low energy consumption. This paper describes a group of circuit partitioning, placement and synchronization methodologies that permits the implementation of excessive speed, low power circuits synchronized with the resonant rotary clocking generation. Resonant rotary clocking era inherently helps (and calls for) non-zero clock skew operation, which permits in addition advanced circuit performances. The proposed physical layout waft involves included circuit partitioning and location methodologies that allow the hierarchical utility of non-0 clock skew machine timing. This layout glide is proven to be a computationally green implementation method.

I. INTRODUCTION

Accomplishing controllable-skew, low-jitter synchronization with low energy dissipation is a primary milestone for virtual synchronous very-massive-scale integration (VLSI) circuits working at better frequency regimes. To attain this milestone, designers may additionally use opportunity methodologies, consisting of a couple of clock domains or wi-fi [1] and transmission line-based totally [2-5] clocking technology. These technologies should be supported by way of particular layout flows and pc-aided layout (CAD) suites with a purpose to be viable in semiconductor implementation. on this paper, a physical design drift for circuits synchronized by means of a transmission line-primarily based clocking technology the resonant rotary clocking generation [5,6] is described. This paper is prepared in follows. In section II, a short evaluate of resonant clocking technologies is provided. In segment III, the proposed physical design methodology is described. In segment IV, experimental results of for various levels of the proposed bodily design drift are presented. Conclusions are counseled in phase V.

II. RESONANT CLOCKING

The winning methodology to generate excessive-frequency clock signals is to use on-chip frequency multiplication with phase-locked loop (PLL) additives. The on-chip PLL additives occupy chip region and result in problems with signal reflections, capacitive loading and strength dissipation that efficaciously restriction the most working frequency. also, in nanoscale complementary-metal-oxide semiconductor (CMOS) technology, the distribution of the clock sign from a unmarried clock supply over a clock tree network [7] has come to be pretty blunders-prone due to sign integrity issues. The resonant clocking technology [2-6] gift an opportunity to generating the synchronizing clock sign thru putting off the necessity to use a complex on-chip PLL component. The implementation of resonant clocking technologies requires long interconnects on the chip, which might be modeled via transmission traces. Rather than the lossy RC characteristics of lengthy wires, (R) LC traits of transmission strains provide the bodily medium for oscillation. A common signal is excited and saved oscillating on transmission traces, which constitutes the worldwide clock signal.

There are three most important varieties of resonant clocking technology presented to date. Those resonant clocking technology are categorized with admire to their oscillator kinds:

 1) Coupled LC oscillator primarily based clocking

2) Standing wave oscillator based clocking [3,4],

3) Traveling wave oscillator primarily based clocking [5, 6].

 Coupled LC oscillator based totally resonant clocking generation presents a steady significance clock sign with a steady segment. Such houses are just like those of a conventional clocking generation. Therefore, the principle gain of coupled LC oscillator based totally resonant clocking technology over different resonant clocking technology is the minimal exchange to the conventional bodily design drift.

Better circuit performances are plausible totally by way of replacing the conventional clock distribution network with that of the coupled LC oscillator primarily based resonant clocking generation.

Status wave oscillator based resonant clocking technology affords a varying amplitude clock sign with a consistent section. just like coupled LC oscillator primarily based resonant clocking generation, the clock phase is consistent, hence, this technology does not require drastic changes to the conventional physical layout flow. touring wave oscillator based resonant clocking technology is the resonant clocking era of interest on this work.

Touring wave oscillator primarily based resonant clocking generation, additionally called rotary clocking generation, offers a clock sign which has a consistent significance and varying segment. varying segment (delay) of the clock signal lets in easy implementation of non-zero clock skew structures. Such structures allow progressed circuit performances [8].

A. Rotary (Traveling Wave Oscillator)

Clock Rotary visiting-wave oscillators (RTWO's) incorporate a next-era clock community implementation generation providing controllable-skew, low-jitter, GHz variety clocking with fast transition instances and occasional energy consumption [5]. RTWO's are generated on move-linked transmission strains, building a differential LC transmission line oscillator. these oscillators generate multiphase square waves with low jitter and controllable skew (360 ranges). multiple RTWO's can be connected together forming the rotary oscillator arrays (ROA) that is the clock distribution community for the rotary clocking era. The primary ROA structure is shown in figure 1 ([5]). This association produces a clock sign**.**
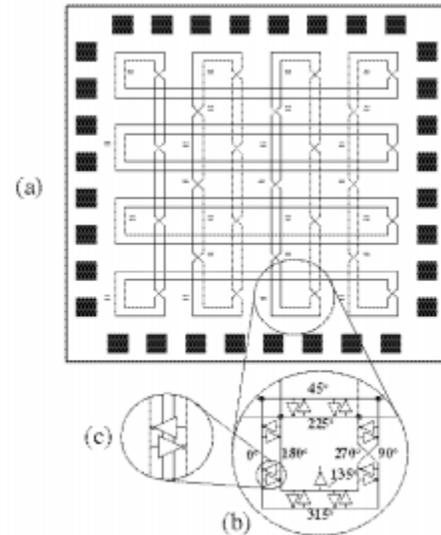

Fig. 1. Basic rotary clock architecture.

in each ring which sweeps around the ring in a frequency depending on the electric period of the ring. Pulses on each ring are segment-locked via the shared transmission line wires between the earrings.

due to the ring shape of ROA's, the clock segment required to synchronize a synchronous element can be decided on with pleasant granularity of skew [up to 360 degrees as shown in Figure 1(b)]. The clock segment using a synchronous component is determined by using the location of the relationship factor of the clock signal cord on the ROA ring.

The anti-parallel inverter pairs [Figure 1(c)] are used among the go-connected strains to keep power, initiate and maintain the visiting wave. After excitation, the anti-parallel inverters feed the travelling wave within the stronger direction, up to a strong oscillation frequency. The dissipated electricity at the ring is given by way of the I2R dissipation in preference to the traditional CV2f expression. that is so due to the fact the energy that is going into charging and discharging.

MOS gate capacitance (of the inverters) will become transmission line strength, which in flip is circulated inside the closed electromagnetic direction.

The operation of the ROA shape carried out in 2.five V zero.25 ,um CMOS technology oscillating at various frequencies such as three.4GHz as a new clocking generation is confirmed by means of simulations in [5]. Promising outcomes of 5.5

playstation clock jitter and 34-dB electricity deliver rejection ratio (PSRR) are measured.

other very important metrics (for any oscillator) are the sensitivity to adjustments in temperature and supply voltage. it has been proven that the frequency deviation with temperature change between -50°C and one hundred fifty°C is only 1% while the alternate with VDD deviation between 1.five and three.5 V is round 2%. The immunity of the RTWO indicators to process versions while allowing complete skew control over 360 ranges of stages at the ring proves very valuable for deep sub micron programs.

B.   Timing Requirements of Rotary Clocking

it is recognized that in spite of the problem in presenting multiphase, non-zero clock skew synchronization with conventional clock generation methodologies, such systems are advanced as compared to the conventional 0 clock skew, single-section structures in permitting better clock frequencies and advanced tolerance to process versions [8-11]. Rotary clocking technology easily substances such multi-segment clocking with a pleasant grain of clock delays (non-0 clock skew).

From a CAD attitude, non-stop delay fashions are used to version clock delays to be had in the network. From a circuit design perspective, the challenge of different clock delays to the synchronous components of a rotary-clock synchronized circuit are crucial for a enormously uniform clock loading. in order to hold the synchronization of an original zero clock skew circuit with rotary clocking, all synchronous additives ought to be driven by using the identical vicinity on the ROA rings. one of these load distribution may additionally have an effect on the rotation of the oscillatory sign on the ring, thereby inflicting degradations within the exceptional of synchronization. additionally, because of simultaneous switching of synchronous additives, this form of distribution may cause thermal hot spots at the chip area. in the most efficient scheduling scenario, the clock delays on the synchronous additives are dispensed relatively calmly in time, main to a fantastically balanced distribution of the latching points on the rotary ring. the required balanced loading of the ROA earrings can be supplied with the aid of clock skew scheduling [8].

Following from the discussions above, it's far stated the implementation of circuits synchronized with the rotary clocking era now not only supports however also calls for the use of nonzero clock skew, multi-

segment synchronization schemes. Such circuits benefit from both the advanced timing methodologies and the rotary clocking generation.

III. DESIGN METHODOLOGY

Synchronization of digital VLSI circuits with the rotary clocking era and the integration of non-0 clock skew, multi-segment design into the circuit layout waft require methodical advent. in this section, these new design paradigms are outlined from the bodily layout and electronic layout automation points of view..
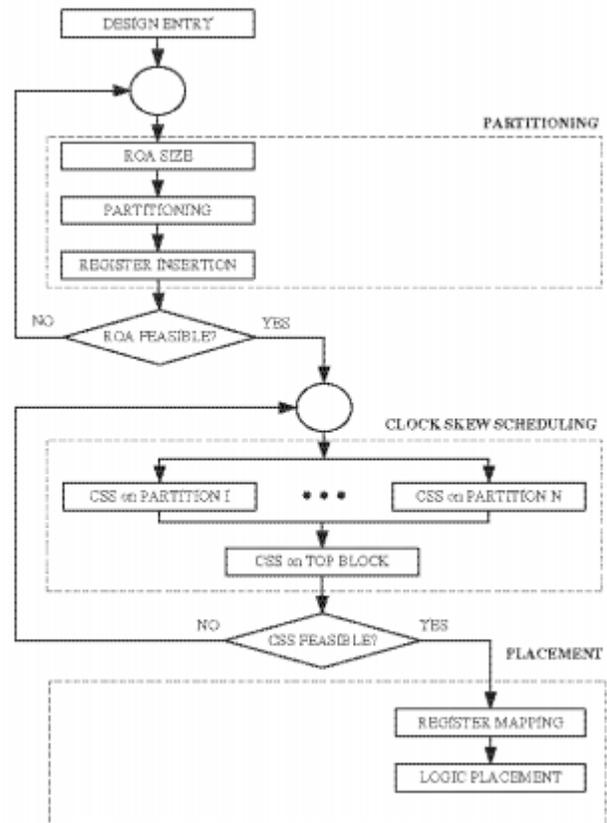

Fig. 2. A go with the flow chart for the physical layout glide of digital VLSI circuits synchronized with the resonant rotary clocking era.

The proposed physical design flow is illustrated with the flow chart in Figure 2. The flow includes processing the layout entry to research the complexity and requirements of the circuit, partitioning the netlist, acting clock skew scheduling and appearing sign in and logic placement.

 The implementation of the ROA jewelry and netlist partitioning are interdependent as illustrated within

the Partitioning step within the drift chart. the size and variety of earrings inside the ROA systems depend upon elements along with the complexity of the layout, the availability of clock network design assets, the computational resources for timing analysis, and the supply of silicon region. notwithstanding these dependencies, the variety and dimensions of ROA earrings in a circuit are quite flexible. The number of ROA jewelry is generally held sufficiently high if you want to restrict the total wire duration. The shapes of ROA rings aren't always ordinary (e.g., rectangles) as implied via the mesh shape defined in section I1-A. Such flexibility in the bodily implementation of the ROA rings allows reconciliation of the non-routable blocks of the chip place.

Partitioning is done on a gate-stage or a check in-toregister level netlist. For the former case, it is regularly necessary to insert more registers in the logic network as a part of the timing-driven partitioning method. This system is represented by means of the "register Insertion" block in the flow chart. those inserted registers are stage-sensitive latches working in the transparent levels of operation with a view to keep the capability of the authentic circuit. The feasibility of the partitioning end result is checked at the following validation step. The partitioning step of the layout drift is repeated as vital.

within the clock skew scheduling (CSS) step, the rotary clock network is constructed. An preliminary timing statistics of the circuit is essential for the application of clock skew scheduling. This records may be acquired by way of acting static timing analysis on a initial placement and routing or a silicon virtual prototype of the circuit. In CSS, information paths which can be local to each partition are recognized and the corresponding timing constraints areincluded inside the clock skew scheduling trouble for that partition. in addition, the timing constraints of local statistics paths which span distinct partitions are blanketed inside the clock skew scheduling hassle of the so called top block. A heuristic approach is proposed to solve the partition and pinnacle block LP problems.

At the position step, the most efficient clock delays at each synchronous component are recognised. Depending at the range of clock phases and the number of registers for a given clock phase, the mapping of synchronous components to the registers inside an ROA ring is executed. that is an automated design step known as "sign up Mapping" inside the waft chart. The relaxation of the common sense

within a partition is placed inside the location to be had within the ROA earrings for this partition. This placement is executed the usage of traditional common sense placement strategies.

These three essential steps of the proposed bodily layout drift are explained in element in the following subsections.

A.   Timing-Driven Partitioning

conventional timing-pushed partitioning strategies thus far are categorised as course-based totally and internet-based totally partitioning, each aiming to restrict the weight of cuts for circuit placement methods [12]. An alternative partitioning approach is proposed right here with choice criteria that results in partitions which can be amenable to non-zero clock skew operation, each synchronized under an ROA ring. In implementation, a partitioning device Chaco [13] from Sandia national Laboratories is used.

 a few of the criteria hired in partitioning are the weight, quantity and region of the cuts, the relative assignments of sequentially-adjacent registers to partitions and the number of inner vertices according to partition. For the walls to be amenable to non-0 clock skew operation, the walls are heuristically enforced to be registered-input and registeredoutput systems.

To make certain this kind of assets, the fanin paths of synchronous components are assigned low area weights. The partitioning device minimizes the reduce weights, leading the cuts to skip via the statistics inputs terminals of synchronous components. A synchronous issue at the border of two walls is visualized as shared between walls, structuring the registered-enter and registered-output scheme. The Chaco partitioning tool may be operated with exceptional priorities assigned to a couple of standards. A balanced precedence assigned between minimizing the total cut weight and growing the quantity of inner vertices in all partitions is selected.
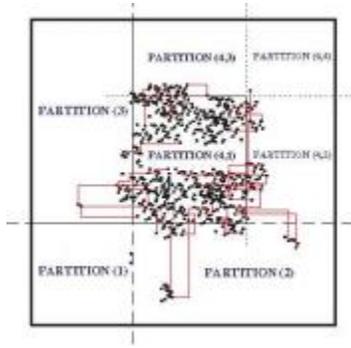
Fig. three. Partitioning a circuit for timing analysis. The black dots represent registers and the strains constitute the information paths.

The information paths which can be on a reduce are identified and the timing analysis on these paths are accomplished on the better hierarchical scale. a few paths from partition (4,1) are confirmed.

Experimentally, this option is found to be sufficiently powerful. The range of internal vertices being excessive, as opposed to having a high wide variety of border vertices among walls, increases the extent of independence of the clock skew scheduling processes on every partition. For RTL-stage netlists, the partitioning application may validate a cut on a internet that is among combinational additives. In such times, "sign up Insertion" is used to fulfill the registered-enter, registered-output scheme. The range of inserted registers depends on the great of the partitioning tool and the complexity of the layout. therefore, in designs where die location is a strict useful resource, the partitioning step need to be carried out with warning. the general partitioning manner is illustrated in discern three.

B.   Non-Zero Clock Skew Scheduling

Due to the registered-input, registered-output partitioning scheme, the clock schedules of partitions may be computed rather independent of each other. Inside the proposed approach, first the clock time table of each partition is computed the use of a traditional clock skew scheduling method consisting of the method in [8,9]. Then, the clock agenda of the top block is computed on the way to make sure compatibility of individual blocks. This heuristic approach does now not assure optimality, however, leads to smaller clock skew scheduling issues (in keeping with partition and top block). Incompatibilities of the outcomes are corrected with iterations. inside the iterative system, both clock skew scheduling of necessary blocks are repeated, or

postpone padding is used to adjust the timing of one or more blocks. those iterative approaches aren't explained or experimented with in this paper due to the validity of the outcomes in demonstrating the feasibility of the design float without such iterations.

C.   Timing-Driven Register Placement

Inside the sign up placement method, specified areas for sign in placement are reserved under the ROA rings. exceedingly populated sign in banks are stacked interior these detailed regions, to be had to be used with the whole spectrum of clock phases. Upon synthesis of the circuit and the computation of most reliable clock phases, each check in within the synthesized netlist is bodily mapped to a register underneath the ROA ring. to complete the position step, the synthesized blocks of combinational circuitry are allotted within the loose area within the vicinity, outside the distinctive regions.

IV. EXPERIMENTAL RESULTS

The development of a layout tool following the pointers of the offered design method is achieved in C and C++ in an open supply surroundings. results for some of the crucial man or woman additives are supplied, demonstrating the feasibility of the proposed bodily layout glide.

 The Chaco partitioning software is tested on real and artificially generated circuits with numerous netlist sizes. specified results are mentioned for the ISCAS' 89 benchmark circuits and for one commercial circuit industriall. the commercial circuit industriall has 107875 circuit components (including 14031 synchronous additives), which include 65908 components for good judgment functionality (closing additives are for test functions). direction enumeration of industrial 1 cannot be completed within the available computing sources. consequently, gate-stage partitioning is carried out on industriall. The ISCAS'89 benchmark circuits are sufficiently huge, but, course enumeration may be effectively carried out on these circuits. for this reason, partitioning is carried out to the check in-to-sign in degree netlist for these circuits. The partitioning results for

•   ISCAS' 89 benchmark circuits, with sign in-to-register level netlist partitioning,

•   Industriall circuit, with gate level netlist partitioning,are reported on a PowerMac pc with twin G5 1.8GHz microprocessors and 3GB RAM running Mac OS X.

A good way to profile the variety of inserted registers for distinctive partition sizes, experiments are done on industriall. As discussed in section III-A, the partitioning step favors the number of interval vertices to be high and range of boundary vertices to be low. additionally, the set sizes have to not be heavily unbalanced for proper synchronization (section II-B). The facts of partitioning industriall into grid sizes of 2x2, 4x4, 5x5, 6x6 and lOxIO by way of Chaco are offered in table I. it's far found that as the number of partitions will increase, the range of registers that want to be inserted on edges (for non-sign in enter cuts) will increase. For a 5x5 sized partition, thenumber of inserted registers (13903) strategies the unique quantity of registers within the circuit (14031). In fashionable, it's miles crucial to choose the dimensions of partitions (wide variety of ROA jewelry) nicely by using considering the scale of the circuit to save you such impractical occurrences.

TABLE I
INDUSTRIAL1 PARTITIONING STATISTICS.

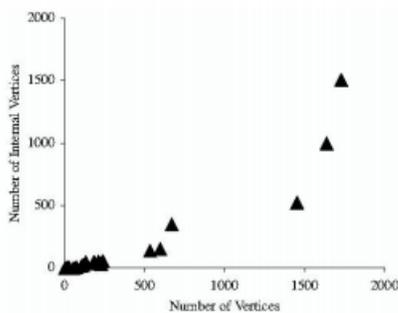| Partition Size	2x2	4x4	5x5	6x6	10x10
# Internal Verts	59393	49385	45616	42857	27787
# Boundary Verts	6515	16523	20292	23051	38121
# Inserted Regs	3011	9751	13903	16172	32131
Run time	15s	23s	28s	32s	54s

Fig. 4. Quality of partitions for ISCAS'89 circuits.

For ISCAS'89 suite of benchmark circuits, partitioning is performed at the check in-to-sign up stage netlist, consequently, register insertion isn't important. The clock skew scheduling troubles of the partitions are solved such that most excellent answers are received, which lead to about 30% shorter clock periods on average as compared to standard, 0 clock skew, edge-brought on circuits (as anticipated, same

to those pronounced in [8]). total run time of the clock skew scheduling system is progressed 28% on common on four processors, wherein the largest circuit (s38417) calls for 1845 secs (in preference to 7707 secs for conventional software 76% improvement). The high-quality of partitions acquired for ISCAS' 89 suite of benchmark circuits is proven in figure 4. note that in the perfect state of affairs, the wide variety of internal vertices have to be identical to the entire quantity of vertices. The run times for Chaco are quite small, with the most important ISCAS'89 benchmark circuit s38417 (1636 registers and 28082 paths) taking 1.28 seconds to partition into four (4) partitions. overall, Chaco generates walls which are nicely perfect for clock skew scheduling in reasonable run times.

In parent five, one of the ROA rings of a regular circuit designed with a zero.thirteenym era on a 2mm x 2mm circuit die is illustrated. The die location is frivolously divided into 16 regions in a four by 4 putting (not proven), every of which is synchronized with an ROA ring. the scale of every ROA ring is 500,um by means of 500,um. inside the zero. 13,m era, a length of a check in is taken into consideration four,um via four,um, with a minimal spacing of two,um between times. consequently, there may be sufficient space to area approximately 80 registers on each ROA ring facet [(500 + 2) /(4 + 2) - 80] for a single row of registers. For four sides of an ROA ring and sixteen jewelry, a complete of 5120 registers are to be had for

mapping against the synthesized logic. This number is adequate for most state-of-the-art digital circuit designs of similar die size. The dimensions of the designated area for register placement and the number of register bank rows are the determining factors for the number of registers in a design, which can be altered for particular design budget requirements. Availability of registers in the register bank enables a good distribution and mapping of clock phases to the synchronous components of a circuit.
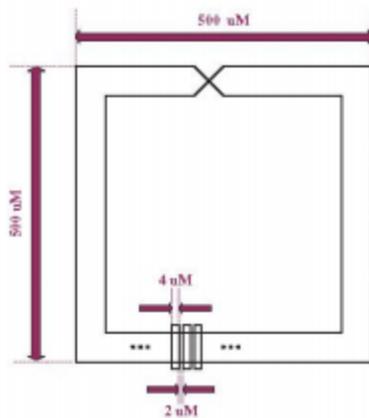
Fig. 5. Illustration of an ROA ring in a chip layout.

V. CONCLUSIONS

In this paper, a bodily layout methodology for timingdriven bodily layout of virtual VLSI circuits with resonant clocking is added. The method steps were established to be useful and green, main to each speedups in execution run time and upgrades in the performance of designed circuits.

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