HIGH-SPEED AND AREA EFFICIENT CONFIGURABLE PARALLEL ADDER FOR APPROXIMATE COMPUTING

[1]K. GOPALAKRISHNA CHOWDARY, [2]V.VENKATA RAO, [3]V. RAMA KRISHNA REDDY
[1]PG scholar, Dept of ECE, Narasaraopeta Engineering College, Guntur District, AP, India
[2]Professor & Head of Dept of ECE, Narasaraopeta Engineering College, Guntur District, AP
[3]Asst.Professor, Dept of ECE, Narasaraopeta Engineering College, Guntur District, AP, India

ABSTRACT: In this paper the implementation of high speed and area efficient configurable parallel adder for approximate computing is done. Basically, adders plays very important role in DSP and micro processor applications. The entire configurable parallel adder structure is divided into three stage, they are pre processing stage, carry generation stage and post processing stage. The array generation stage plays very important role in entire system. From results it can observe the RTL schematic, Technology schematic of configurable parallel adder. Hence the configurable parallel adder gives effective results.

KEY WORDS: Approximate computing, carry mask able adder, parallel adder, RTL (Register Transfer Level), CMHA (Carry Mask able Half Adder).

I. INTRODUCTION

Basically, in VLSI chip design signal processing is implemented for effective integration in the system. In present generation, integration plays major role to get effective output. In signal processing applications the capacity of signal is computed [1]. In VLSI design mainly energy and area plays important role in the entire system. Two main forces are required to reduce the energy consumption. The operating frequency and chip capacity is operated in the system for the purpose of growth. By using cooling techniques the energy consumption is determined.

In electronic devices the battery life plays important role in the system. There will be a limitation for battery life and the operation time is also prolonged in the entire system.

In signal processing algorithms, multiplication operation plays important role in entire system. By using adders, energy and latency is considerable. In VLSI design, adder gives low energy consumption. Logic levels and circuit in multipliers is extended and area is consumed. To perform high speed operations, multipliers are arranged in parallel form. Adders are classified based on two multipliers. They are fully parallel adders and fully serial adders [2]. Various bits are operated using single digit serial multiplier. Here by using this, both area and speed is operated at highly.

In digital computers and digital signal processor, the addition operation is performed effectively. Arithmetic operations are performed in basic building blocks which plays major role in entire system. In hardware architecture, arithmetic unit plays major role and process of addition operation is easily performed. Different characteristics and different architectures are existed to perform the arithmetic operations. Binary adder structure is implemented and compared with various analysis [3-4].

The configuration of adders are classified into various types they are Ripple carry adder, carry skip adder, carry look ahead adder and carry select adder. Carry skip optimization algorithm is introduced to map the problems occurred in the system. Multi level tree structures are implemented in the carry skip optimization technique. This will fix the length of modules in the system. This will optimize the number of levels, number

of sizes and number of blocks. Carry signals are carried to increase the speed of the buffers. CMOS will implement the logical configurations in the narrow fields. Static and dynamic gates are implemented to limit the operations of binary adders [5].

II. RELATED WORK

a. BINARY ADDITION

Binary addition performs the addition process based on the logic gates. Here single or two bit binary numbers are used. In binary addition process sum and carry are the outputs.

b. SERIAL ADDER

Bit serial adder is the name of serial adder. Binary addition operation is performed in serial adder. Carry out and sum is the two outputs which are also single bit. Addition is executed by adding each bit from least significant bit to most significant bit and each bit has one clock cycle.

Full adder and one flip-flop are used in serial binary adder. Carry out signal for every clock cycle is given into flip flop. Thus the flip-flop generates the output as carry-in signal for next clock cycle. After completion of all bits of input operand, all bits of sum come from sum output.

1. The serial adder contains two binary digits along with carry bit from previous addition. Clock input will trigger the every addition.

2. By using carry reset pin R, carry bit from addition at previous clock pulse is set to zero.

3. The output can be complement of sum in some serial adders, it is optional.

Serial adder is a digital circuit which is a sequential circuit which contains full adder and flip-flop. At every clock cycle, previous bit addition result is taken and flip-flop stores the carry from full adder. Sum result is calculated and carry is given to flip-flop for next calculation. In this way, input data is given to full adder in serial format and it is synchronised by clock.

c. BCD ADDER

BCD (binary coded decimal) adder is a digital circuit in which two BCD numbers are added in parallel form and carry out & sum bits are generated. The result of sum will not be in BCD form when addition of two BCD digits is done.

The BCD result is correct in first example and BCD result is not correct in second example. BCD digits are represented from 0 to 9. To represent BCD numbers, four bits are required. But by using four bits, 16 values are represented. In the BCD digits extra six values are ignored because BCD digits are represented from 0 to 9. After addition, the result will not in BCD form when the result is greater than 9. It contains corrections to be done to obtain correct BCD results

III. EXISTED SYSTEM

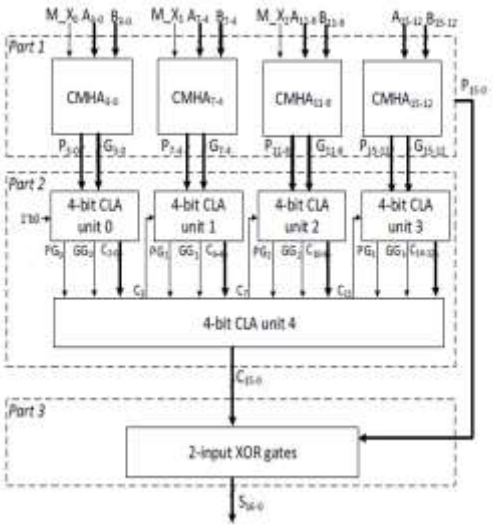

Fig. 1: EXISTED SYSTEM

The above figure (1) shows the architecture of existed system. The existed framework structured a precision configurable adder by concealing the carry proliferation at runtime. This adder accomplishes the first reason for carrying a fair-minded advanced outcome among force and deferral without giving up

precision. The CMHA, which is a productive adder as far as force utilization and territory use, was presented. The basic way deferral of the CMHA is a lot littler than the one in the RCA, while its territory and force utilization are like those of the RCA. Furthermore, the power delay product (PDP) of the CMHA is littler than those of the CLA and PPA structures. Furthermore, because of the modest number of transistors, the CMHA profits by generally short wiring lengths just as a customary and basic format.

The similarly lower speed of this adder structure, in any case, restricts its utilization for rapid applications. In this paper, given the highlights of the CMHA structure, we have concentrated on diminishing its deferral by adjusting its execution dependent on the static CMHA rationale. The fixation on the static CMOS starts from the craving to have a dependably working circuit under a wide scope of gracefully voltages in exceptionally scaled innovations. The existed alteration speeds up significantly while keeping up the low zone and force utilization highlights of the CMHA. Furthermore, an alteration of the structure, in light of the variable idleness procedure, which thus brings down the force utilization without significantly affecting the CMHA speed, is additionally introduced. As far as we could possibly know, no work focusing on plan of CMHAs working from the super edge district down to approach limit area and furthermore, the structure of (half breed) variable inertness CMHA structures have been accounted for in the writing.

IV. PROPOSED SYSTEM

The below figure (2) shows the structure of parallel adder. Basically, the entire block diagram is divided into three stages; they are pre-processing stage, carry generation stage and post processing stage. The pre-processing stage generates the propagate and generate signals. The carry generation stage is controlled by the intermediate signals. At last the post processing stage gives output as sum.

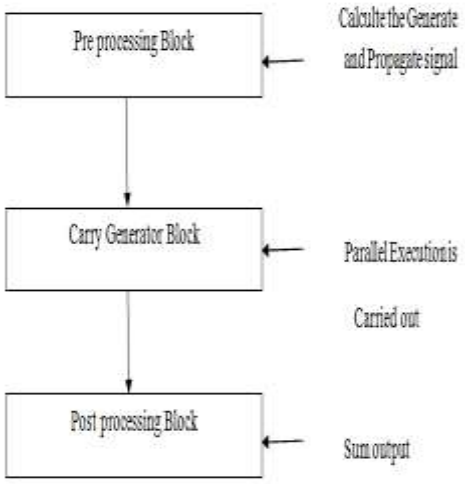

Fig. 2: STAGES IN PROPOSED SYSTEM

Three stages are presented in the configurable parallel adder is explained in detail manner.

1. Pre-Processing Stage:

In this stage, propagate signals and generate signals are manipulated to pair of each inputs A and B. Propagate signal and generate signal are represented as

$$Pi = Ai \text{ XOR } Bi$$
$$Gi = Ai \text{ AND } Bi$$

2. Carry Generation Network:

In carry generation stage the calculation is performed based on the bits and carries obtained. The entire operation is performed in the form of parallel. Generate and propagate signals are obtained from the intermediate signals. The below equations shows the propagate and generate signals:

$$Pi{:}j = Pi{:}k \text{ AND } Pk\text{-}1{:}j$$

$$Gi{:}j = Gi{:}k \text{ OR } (Pi{:}k \text{ AND } Gk\text{-}1{:}j)$$

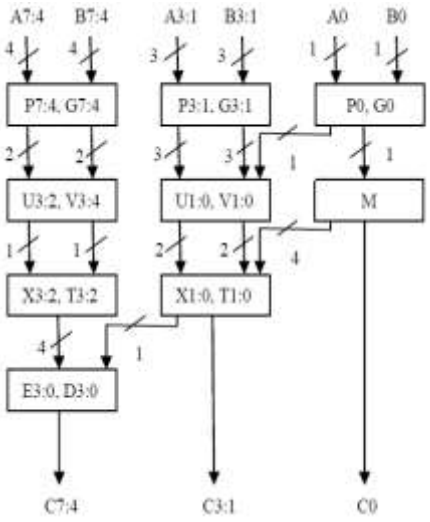

Fig. 3: PROPOSED SYSTEM

3. Post Processing Stage:

In post processing stage the calculation is performed based on the input bits. From post processing stage sum and carry is generated. The below equations shows the sum and carry equations:

$$Ci = (Pi \text{ AND } Cin) \text{ OR } Gi$$

$$Si = Pi \text{ XOR } Ci\text{-}1$$

In applications of high speed circuits, very useful adder is configurable parallel adder. Configurable parallel adder is designed based on the power and area.

Structure delay= $\log_2 n$

Number of computation nodes= $[(n)\ (\log_2 n)\text{-}n+1]$

The fan-out problem is recognized by parallel adder and recursive doubling algorithm is introduced. Idem potency property is used in configurable parallel adder which controls the fan-out. Cost is increased due to number of lateral wires at every stage. Here massive overlap is occurred between prefix sub-terms. Hence, the implementation of configurable parallel adder occupies less area.

V. RESULTS

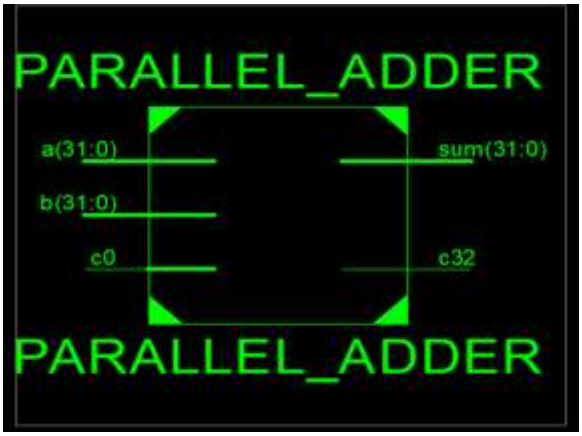

Fig. 4: RTL SCHEMATIC

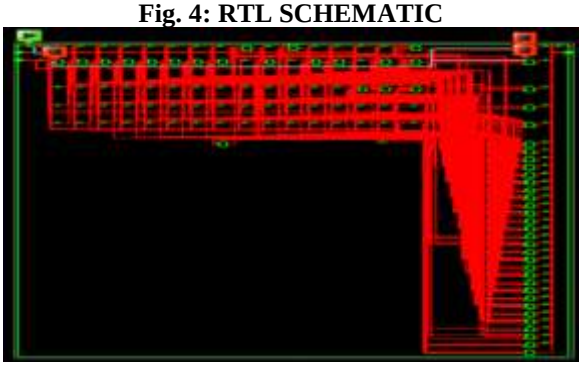

Fig. 5: TECHNOLOGY SCHEMATIC

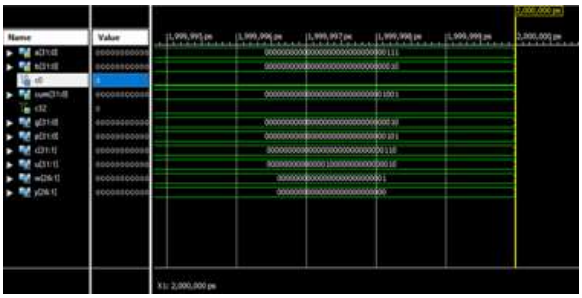

Fig. 6: OUTPUT WAVEFORM

VI. CONCLUSION

The paper gives the design and implementation of configurable Parallel adder using approximate computing. Configurable Parallel Adder is perform its operation in parallel form, because of this there will be increase in the speed of operation. Configurable parallel adder performance mainly depends on prefix-processing stage. Parallel adder can decrease the number of black cells. Hence

configurable parallel adder gives effective results.

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K.GOPALAKRISHNA CHOWDARY Completed B.Tech from Lovely Professional University, Punjab and pursuing M.Tech in Narasaraopeta engineering college, A.P, India. His M.Tech specialization is Digital Electronics and Communication Systems.

V. VENKATARAO Completed B.Tech from B.L.D.E.A's College of Engineering and Technology, Bijapur of Karnatak University and M.Tech from University College of Engineering, Osmania University, Hyderabad and Ph.D in the area of GPS from JNTUH, Hyderabad. At present he is working as Professor in Narasaraopeta Engineering College, A.P, India.

V. RAMA KRISHNA REDDY Completed B.Tech from Sri Padmavathi Engineering College, Madras University and M.Tech from Balaji Institute of Technology & Science, JNTUH. At present he is working as Assistant Professor in Narasaraopeta Engineering College, A.P, India