Design Of Low Power And Less Delay Full Adder And Ripple Carry Adder Using MGDI Technique

B.Mounika
Department of Electronics And Communications Engineering(ECE)
Andhra Loyola Institute of Engineering and Technology(ALIET)
Vijayawada, Andhra Pradesh,India.

G.LeelaSravanthi
Department of Electronics And Communications Engineering(ECE)
Andhra Loyola Institute of Engineering and Technology(ALIET)
Vijayawada, Andhra Pradesh,India.

V K R S Ahalya
Department of Electronics And Communications Engineering(ECE)
Andhra Loyola Institute of Engineering and Technology(ALIET)
Vijayawada, Andhra Pradesh,India.

G Ravi
Asst.Prof,Department of Electronics And Communications Engineering(ECE)
Andhra Loyola Institute of Engineering and Technology(ALIET)
Vijayawada, Andhra Pradesh,India.

***Abstract*—In the modern era, processors require more speed and less power consumption circuits for the operation. An Adder is a fundamental building block in any arithmetic applicationand is widely utilised in very large-scale applications(VLSI) like digital signal/image processing and microprocessor applications.Delay,power and area plays an important role in the design of any adder cell.This paper focuses on the design of 8 transistors fulladder. With the help of a fulladder,we can design an n-bit fulladder circuits i.e. a ripple carry adder for multiple bit arithmetic operations using the Gate-Diffusion-Input(GDI) technique.The GDI technique is used for the less power applications as the number of transistors can be reduced to design any application. The proposed design is simulated using the Tanner tools v13.00 at 250nm technology. The power analysis and delay report is observed by the Tanner software.**

Keywords—Full adder,Ripple carry adder,GDI technique, delay,Tanner simulator.

I. INTRODUCTION

In this digital era, we prefer the devices with high speed and which requires less power consumption for the operation and then finally which occupies the small area. The Very Large-Scale Integration(VLSI) can be defined as "embedding thousands of IC's on a single chip". So the VLSI technology, mainly focuses on the miniaturization i.e. to get improved performance of the system.In order to miniaturize any circuit we require less number of transistors to perform a specific task. If we design any circuit with less number of transistors, it automatically reduces the power consumption and delay.The task of a designer is to design a circuit which requires less number of transistors without compromising on the results i.e. accurate results should be produced.The VLSI applications like microprocessors,digital signal processing,image or vedio processing uses arithmetic operation widely.This paperfocuses on the idea of designing a Fulladder and 4-bit Ripple adder using GDI technique.

In VLSI technology,the circuit complexity is mainly dependson the number of transistors employed in the design. Inorder to reduce the size i.e. complexity of the design ,we need a circuit with minimum(less) number of transistors. As the transistors employed in thedesign are reduced the power consumed by the transistors reduces and the delay time for switching the transistors On/Off also reduces. Among several optimization techniquesproposed for the low power designs, GDI technique is most preferred for the design of any circuit.The expressions for the CMOS logic for sum and carry is as follows:

$$\text{Sum} = (A \oplus B) \oplus C_{in}$$

$$C_{out} = (A \cdot B) + C_{in} \cdot (A \oplus B)$$

The complementary metal oxide semiconductor(CMOS) technology uses 24 transistors for the design of full adder circuit(1-bit). Inorder to design multi-bit full adder we require more number of transistors, for example if we want to design 4-bit adder circuit we require nearly 256 transistors for the operation.If thecount of the transistors increases in the circuit,thedelay and the power consumption increases.By using the GDI technology , we can reduce the transistor count and other parameters also gets improved.

II. INTRODUCTION TO GDI TECHNOLOGY

In this digital era, we prefer the devices with high speed and which requires less power consumption for the operation and then finally which occupies the small area.In the Very Large-Scale Integration(VLSI) there are many technologies which are improving the performance of various devices. One of the best techniques to reduce the count of the transistors and the power consumption is GDI technique.The GDI can be abbreviated as Gate Diffusion Input.The GDI is built up of a basic primitive cell which consists of a single P-mos and N-mos transistors which is similar to CMOS inverter structure. The primitive of GDI cell consists of 4 terminals namely, G,P,N and OUT .The terminal description is as follows:G-commoninput for the gate terminals of both transistorsi.e PMOS as well as the NMOS,P-the drain and substrate terminal of pMOS transistor is connected,N-the outer source and substrate terminal of nMOS transistor is connected,andOut-diffusion node for both pMOS and nMOStransistors as shown in Fig 1.The basic difference which can be observed between the CMOS and GDI is the drain pin of pMOS is connected to input i.e. P instead of supply voltage. Similarly, the sourcepin of nMOS is connected to input i.e. N instead of ground.
The GDI technique was first introduced insilicon fabrication and next usedin thedesign of CMOS standard compatiblecell,introducedto decrease the power consumed by the circuit as shown in the Fig 1.

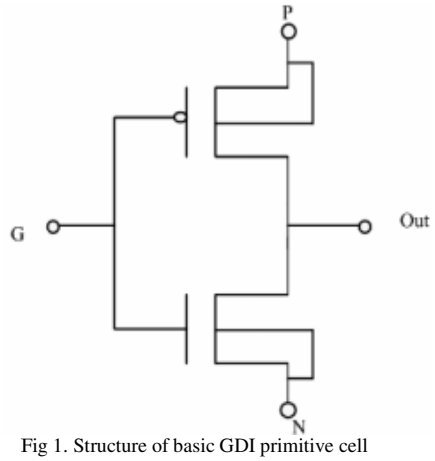

Fig 1. Structure of basic GDI primitive cell

III. OVERVIEW OF EXISTING 14T GDI TECHNIQUE

The normal CMOS technology uses 24 transistors for the fulladderdesign.By using GDI technique,we can reduce the transistor count i.e. with 14 transistors only we can design a full adder circuit as shown in Fig 2.

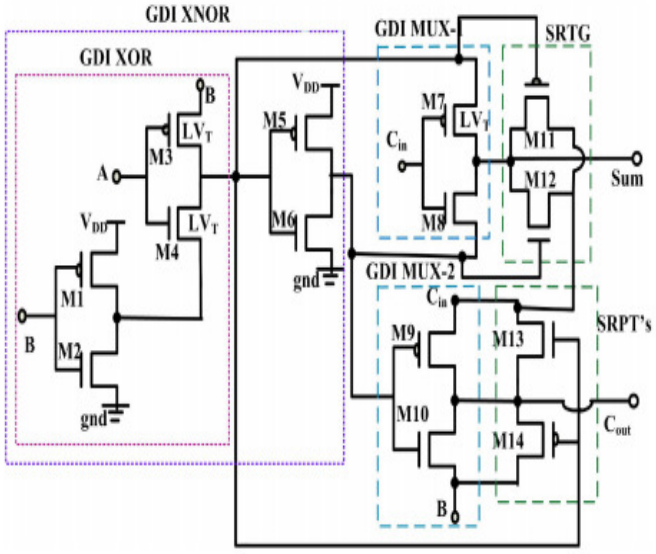

Fig 2. Structure of 14T Full adder design

The expressions(Layout) forsum of the inputs(sum) and carry generation(Cout) for the existing 14T design are given below:

$$\text{Sum} = \overline{C_{in}}(A \oplus B) + C_{in}(A \odot B)$$

$$C_{out} = \overline{(A \odot B)}C_{in} + (A \odot B)B$$

The above 14T design uses XOR-XNOR logic for the construction of a fulladder.The delay(slowdown) and power consumption is reduced compared to the CMOS logic which is using 24 transistors. Here, if we want to design a multi bit adder like 4-bit ripple carry adder we require a minimum of 56 transistors.Comparing to the exixting CMOS logic which uses 96 transistors for the

uses 14T for the full adder design.The 4-bit ripple carry adder is designed using the 14T model as an instance as shown in the Fig 3.Here, we have considered initial carry input i.e.Cin as Gnd(bit-0). We considered 4-bit inputs i.e. A(A0,A1,A2,A3) and B(B0,B1,B2,B3) and output SUM as S0,S1,S2,S3 as shown in the Fig 3. The drawback of the GDI technique is that the substrate of pMOS is connected tothe drainand the substrate of nMOS is connected to the source,which increases the subthreshold current and gate leakage.

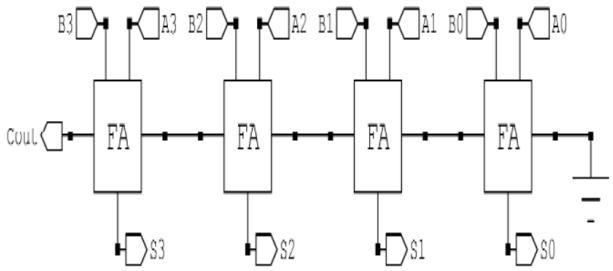

Fig 3.Schematic of Ripple Carry Adder using the Fulladder as an instance.

IV. Overview of Modifiedgdi Technique

The drawback in the GDI technique i.e. subthreshold current and gate leakage can be overcome through Modified GDI technique. The difference between the GDI and Modified GDI technique is that in GDI the substrate of pMOS is connected to the drain whereas in Modified GDI ,thesubstrate of pMOS is connected to the VDD(5V). Similarly, the substrate of nMOS is connected to source in GDI whereas in Modified GDI the substrate of the nMOS is connected to the Ground(0V)inorder to reduce the subthreshold currents and gate leakage. The basic primitive of the Modified GDI is as shown in the Fig 4.Hence,modified GDI is an efficient technique for reducing the number of transistors in the design which inturn reduces the delay and power consumed by the design.

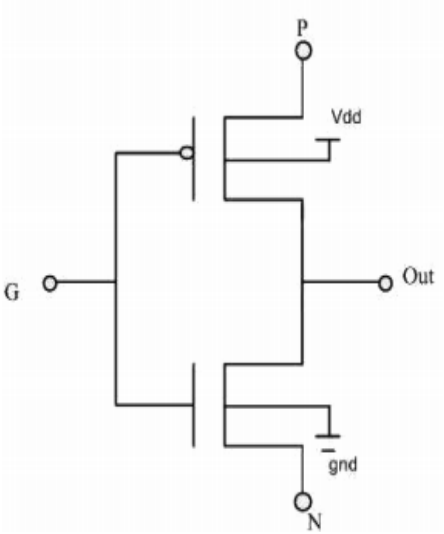

Fig 4. Stucture of basic Modified GDI primitive cell

V. Proposed 8T Modified GDI Technique

As the existing GDI full adder design has 14 transistors,the transistor count has to be reduced inorder to get the efficient results. So the proposed technique uses only 8 transistors for the construction of full adder. Therefore, we can design a 4-bit ripple carry adder with minimum32 transistors whereas in the existing technique the number of transistors used are 56. Therefore,the power consumption and delay automatically gets reduced by using Modified GDI technique. The design of 8 transistors full adder(shown in the Fig 5) and the expressions used for the full adder design are as follows:

$$\text{Sum} = (A \oplus C_{in}) \cdot \overline{C_{out}} + \overline{A \oplus C_{in}} \cdot B$$

$$C_{out} = (A \oplus C_{in}) \cdot B + \overline{A \oplus C_{in}} \cdot A.$$

The 8T full adder produces less delay and the power consumed is also less compared to the conventional GDI full adder design. The subthreshold currents and gate leakage issues can be overcome through an efficient design i.e. using the Modified GDI technique and the simulation results are observed through the Tanner simulator at 250nm technology.Here ,in 8T design we have taken inputs as A,B,Cin and CBAR. We have considered one more input for the fulladder design to achieve the better results. The CBAR is equivalent to $\overline{C_{in}}$.we can consider an inverter without taking CBAR input but the parameters like delay and power

parameters ,we have taken one more input i.e. CBAR in the design as shown in Fig 5. In this design we have used 4 basic primitives of the MGDI to get the efficient results for the fulladder design.

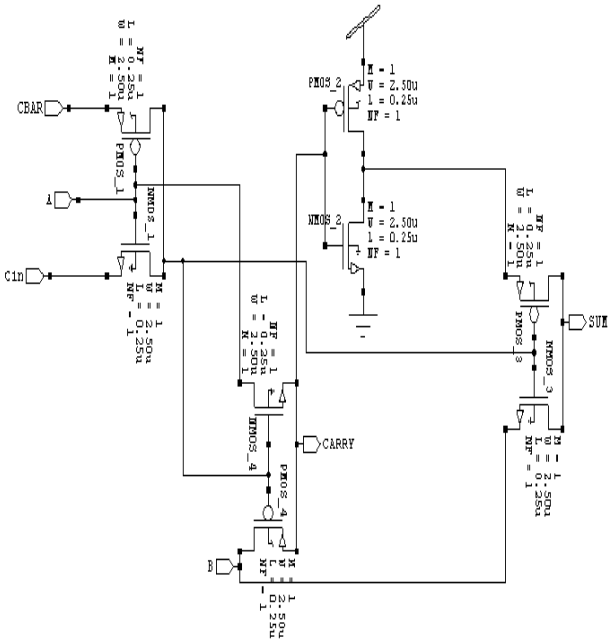

Fig 5. Structure of 8transistorfulladder using Modified GDI

The 4-bit Ripple carry adder can be designed from the 8 transistor Fulladder as shown in the Fig 6.Here,we considered 8transistor full adder as an instance and designed the 4-bit fulladder(4-bit Ripple carry adder). In the full adder design we considered an extra input i.e.CBAR ,so in the ripple carry adder design we have taken 3- inverters for the Cin input to get inverted to obtain the CBAR input from Cin(shown in Fig 6). Here the name of the 8T full adder instance is taken as FAC. We considered the Cin as Gndi.e. bit-0 which results the CBAR as Vdd i.e. bit-1.

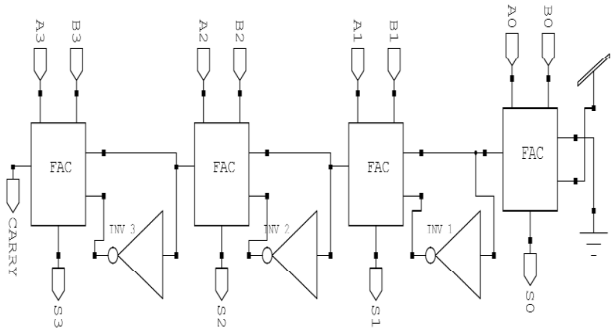

Fig 6. Structure of 4-bit Ripple Carry Adder

The inputs for the design of 4-bit Ripple carry adder are as given below:
A(A0,A1,A2,A3) and B(B0,B1,B2,B3) and output SUM as S0,S1,S2,S3 and CARRY as shown in Fig 6.

VI. SIMULATION RESULTS

The Simulation results are observed in Tanner software using T-spice. To observe the outputs in the T-spice ,we need to write code to apply inputs and also to get the power analysis of the design. The inputsfor fulladder design in t-spice is as follows:
VDD GND 5
A GND BIT ({00001111})
B GND BIT ({00110011})
Cin GND BIT ({01010101})
CBAR GND BIT ({10101010})

As we have discussed earlier the CBAR input is inverted to Cin. Here the ".power" keyword is used to get the power analysis report and the print statement is used to print the list of inputs and outputs in W-edit.
The obtained simulation results are as shown in the Fig 7.

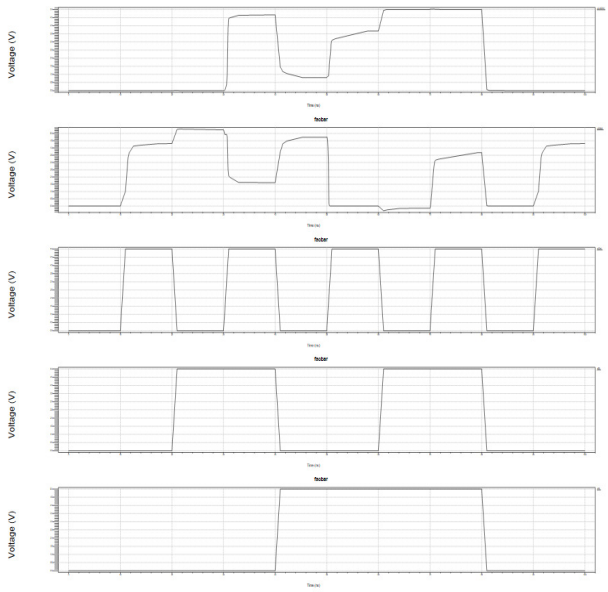

Fig 7. 8T full adder simulation results

The inputs to obtain the results for the 4-bit Ripple adder are as follows:

VDD GND 5
A0 GND BIT ({00001111})
A1 GND BIT ({00110011})
A2 GND BIT ({00110011})
A3 GND BIT ({00110011})
B0 GND BIT ({00110011})
B1 GND BIT ({00110011})
B2 GND BIT ({00110011})
B3 GND BIT ({00110011})

Here the power keyword is used at each node inorder to get the power consumed at each node while calculating total power consumed by the design.

The simulation results for the new(proposed) 4-bit fulladder is observed by W-edit is as shown in the Fig 8.

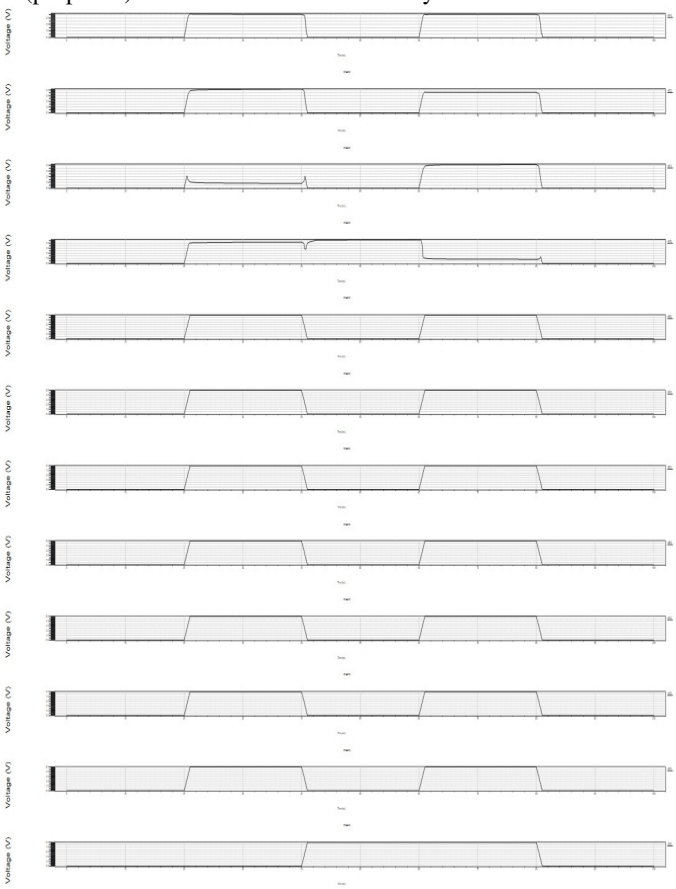

Fig 8. 4-bit Ripple carry adder simulation results

VII. COMPARISON FOR THE EXISTING AND THE PROPOSED MODEL

Based on the design the basic difference between the existing and the proposed technique is as follows:

1. Modified GDI technique used
2. Transistors count reduced
3. Delay and power calculations

The transistor count comparison table for the existing(GDI) and the proposed(MGDI) technique is as follows:

Technique	Full adder	Ripple carry adder
Existing	14	56
Proposed	8	32+3 inverters

The various types of delay considered here are Overhead, DC operating point,setup,Transient Analysis and Parsing.Thedelay comparison table for the existing and the proposed technique is as follows:

Technique	Full adder	Ripple carry adder
Existing(14T)	5.43s	7.44s

The power comparison table is based on the average power power consumption at each node. The power comparison table for the existing and the proposed technique is as follows:

Technique	Full adder	Ripple carry adder
Existing(14T)	5.99e-04 watts	8.88e-04watts
Proposed(8T)	1.88e-04watts	5.41e-04watts

VIII. CONCLUSION

The main objective of this paper is to design a fulladderby usinglesstransistors(only 8) by using MGDI technique. The multi-bit fulladder(i.e. 4-bit)Ripple Carry Adder is also designed by using 8transistorfulladder as an instance in Tanner simulator.There are various techniques used for designing a fulladder but the MGDI technique is preferred to design the circuit as less number of transistorsused.The main objective of designing a full adder with less number of transistors is to reduce delay,power consumption and area also.The proposed method have improved the required parameters.The delay and power consumption is reduced and observed through the Tanner simulator at 250nm technology and the results are tabulated as shown above. In this design we used an extra input CBAR inorder to get efficient results. Thus ,theproposed MGDI technique is efficient and can be used in the VLSI applications where the delay,power consumption and area plays a major role. As the delay increases ,the speed of operation of the various VLSI applications increases simultaneously the power consumption also reduced.

REFERENCES:

[1] IET Circuits Devices Syst., 2019, Vol. 13 Iss. 4, pp. 465-470 © The Institution of Engineering and Technology 2019

[2] abu-Shama, e., Bayoumi, M., 1996. A New Cell for Low Power Adders. IEEE Int. Symp. on Circuits and Systems, p.49-52. [doi:10.1109/iscas.1996.541898]

[3] Bui, H.T., Wang, Y., Jiang, Y.T., 2002. Design and analysis of low-power 10-transistor full adders using novel XORXNOR gates. IEEE Trans. Circ. Syst. II, 49(1):25-30. [doi:10.1109/82.996055]

[4] Wang, D., Yang, M.F., Cheng, W., Guan, X.G., Zhu, Z.M., Yang, Y.T., 2009. Novel Low Power Full Adder Cells in 180nm CMOS Technology. 4th IEEE Conf. on Industrial Electronics and Applications, p.430-433. [doi:10.1109/ICIEA.2009.5138242]

[5] Zimmermann, R., Fichtner, W., 1997. Low-power logic styles: CMOS versus pass-transistor logic. IEEE J. Sol.-State Circ., 32(7):1079-1090. [doi:10.1109/4.597298]

[6] Zackriya, M.V., Kittur, H.M.: 'Content addressable memory-early predict and terminate precharge of match-line', IEEE Trans. VLSI Syst., 2017, 25, (1), pp. 385–387

[7] Bhattacharyya, P., Kundu, B., Ghosh, S., et al.: 'Performance analysis of a low-power high-speed hybrid 1-bit full adder circuit', IEEE Trans. VLSI Syst., 2015, 23, (10), pp. 2001–2008

[8] Navi, K., Foroutan, V., Azghadi, M.R., et al.: 'A novel low-power full-adder cell with new technique in designing logical gates based on static CMOS inverter', Microelectron. J., 2009, 40, (10), pp. 1441–1448

[9] Alioto, M.: 'Enabling the internet of things from integrated circuits to integrated systems' (Springer, New York, 2017, 1st edn.)

[10] Shih-Chieh Chang, Lukas P.P.P. van Ginneken, IEEE Transaction on Computers, Vol. 48, No. 9, September 1999

[11] Rabaey, J.M., Chandrakasan, A., Nikolic, B.: 'Digital integrated circuits: a design perspective' (Prentice Hall, NJ, USA, 2003, 2nd edn.)

[12] Zackriya, M.V., Kittur, H.M.: 'Content addressable memory-early predict and terminate precharge of match-line', IEEE Trans. VLSI Syst., 2017, 25, (1), pp. 385–387

[13] International Roadmap for Devices and Systems (IRDS), 2017 Edition, https://irds.ieee.org/

[14] Navi, K., Moaiyeri, M.H., Mirzaee, R.F., et al.: 'Two new low-power full adders based on majority-not gates', Microelectron. J., 2009, 40, (1), pp. 126– 130

[15] Radhakrishnan, D.: 'Low-voltage low-power CMOS full adder', IEE Proc., Circuits Devices Syst., 2001, 148, (1), pp. 19–24